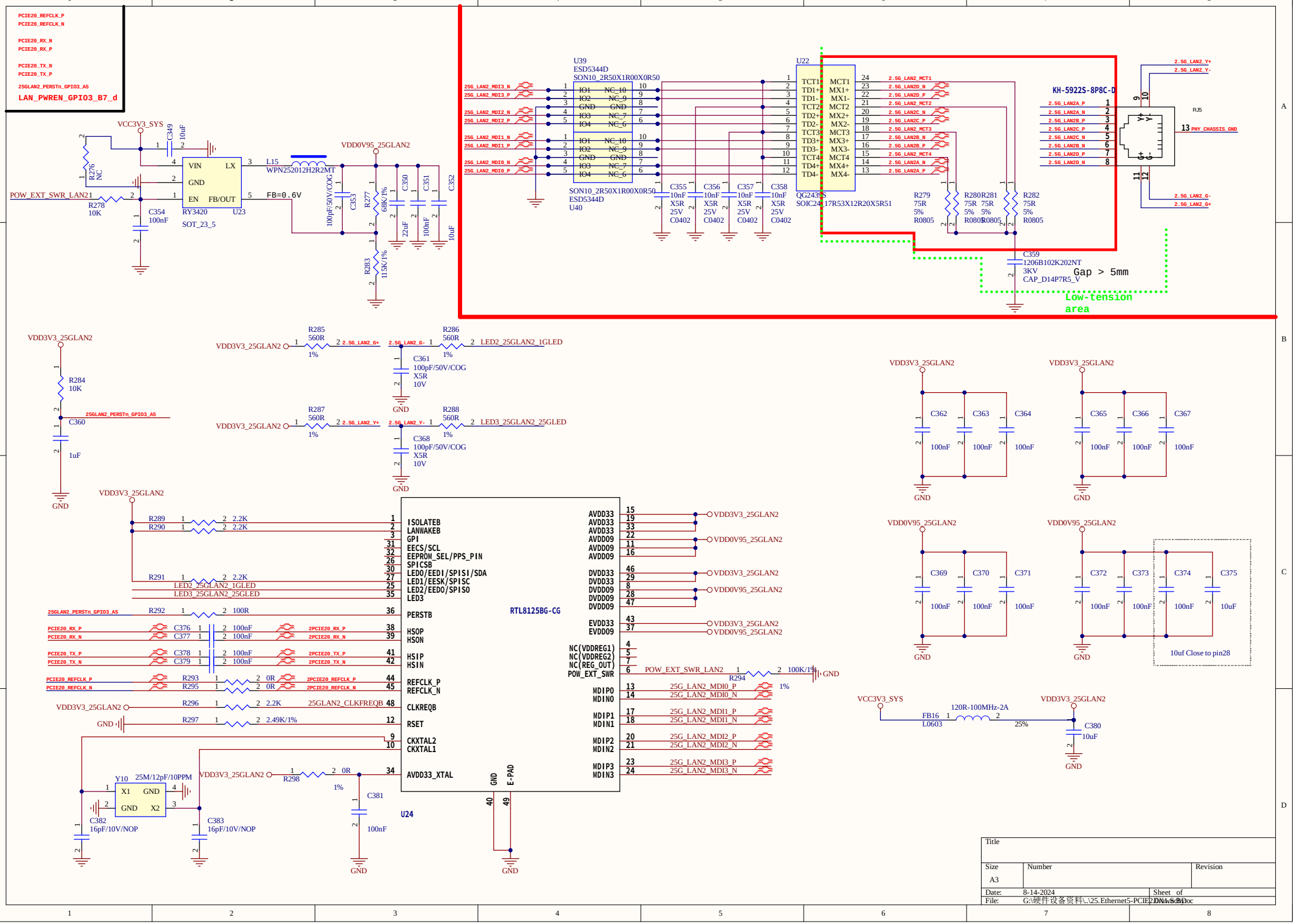
PCIE20_REFCLK_P
PCIE20_REFCLK_N
PCIE20_RX_N
PCIE20_RX_P
PCIE20_TX_N
PCIE20_TX_P
25GLAN2_PERSTn_GPIO3_A5
LAN_PWREN_GPIO3_B7_d
VCC3V3_SYS
C349 10uF
R276 NC
VIN LX GND EN FB/OUT
RY3420 SOT_23_5
U23
L15 WPN252012H2R2MT
FB=0.6V
POW_EXT_SWR_LAN21
R278 10K
C354 100nF
VDD0V95_25GLAN2
100pF/50V/COG
C353
R277 68K/1%
C350 22uF
C351 100nF
C352 10uF
R283 115K/1%
U39
ESD5344D
SON10_2R50X1R00X0R50
SON10_2R50X1R00X0R50
ESD5344D
U40
25G_LAN2_MDI3_N
25G_LAN2_MDI3_P
25G_LAN2_MDI2_N
25G_LAN2_MDI2_P
25G_LAN2_MDI1_N
25G_LAN2_MDI1_P
25G_LAN2_MDI0_N
25G_LAN2_MDI0_P
IO1 IO2 GND IO3 IO4 NC_10 NC_9 NC_7 NC_6
C355 10nF X5R 25V C0402
C356 10nF X5R 25V C0402
C357 10nF X5R 25V C0402
C358 10nF X5R 25V C0402
U22
QG2435 SOIC24_17R53X12R20X5R51
TCT1 TD1+ TD1- TCT2 TD2+ TD2- TCT3 TD3+ TD3- TCT4 TD4+ TD4-
MCT1 MX1+ MX1- MCT2 MX2+ MX2- MCT3 MX3+ MX3- MCT4 MX4+ MX4-
2.5G_LAN2_MCT1
2.5G_LAN2D_N
2.5G_LAN2D_P
2.5G_LAN2_MCT2
2.5G_LAN2C_N
2.5G_LAN2C_P
2.5G_LAN2_MCT3
2.5G_LAN2B_N
2.5G_LAN2B_P
2.5G_LAN2_MCT4
2.5G_LAN2A_N
2.5G_LAN2A_P
R279 75R 5% R0805
R280 75R 5% R0805
R281 75R 5% R0805
R282 75R 5% R0805
KH-5922S-8P8C-D
RJ5
PHY_CHASSIS_GND
2.5G_LAN2_Y+
2.5G_LAN2_Y-
2.5G_LAN2_G-
2.5G_LAN2_G+
C359 1206B102K202NT 3KV CAP_D14P7R5_V
Gap > 5mm
Low-tension area
VDD3V3_25GLAN2
R284 10K
C360 1uF
GND
R285 560R 1%
R286 560R 1%
LED2_25GLAN2_1GLED
C361 100pF/50V/COG X5R 10V
R287 560R 1%
R288 560R 1%
LED3_25GLAN2_25GLED
C368 100pF/50V/COG X5R 10V
C362 C363 C364 C365 C366 C367 100nF
C369 C370 C371 C372 C373 C374 C375 100nF
C375 10uF
10uf Close to pin28
VDD0V95_25GLAN2
R289 2.2K
R290 2.2K
R291 2.2K
R292 100R
R293 0R
R295 0R
R296 2.2K
25GLAN2_CLKFREQB
R297 2.49K/1%
R298 0R 1%
Y10 25M/12pF/10PPM
X1 GND GND X2
C382 16pF/10V/NOP
C383 16pF/10V/NOP
C381 100nF
U24
RTL8125BG-CG
ISOLATEB
LANWAKEB
GPI
EECS/SCL
EEPROM_SEL/PPS_PIN
SPICSB
LED0/EEDI/SPISI/SDA
LED1/EESK/SPISC
LED2/EEDO/SPISO
LED3
PERSTB
HSOP
HSON
HSIP
HSIN
REFCLK_P
REFCLK_N
CLKREQB
RSET
CKXTAL2
CKXTAL1
AVDD33_XTAL
GND
E-PAD
AVDD33
AVDD09
DVDD33
DVDD09
EVDD33
EVDD09
NC(VDDREG1)
NC(VDDREG2)
NC(REG_OUT)
POW_EXT_SWR
MDIP0 MDIN0
MDIP1 MDIN1
MDIP2 MDIN2
MDIP3 MDIN3
R294 100K/1%
VCC3V3_SYS
FB16 L0603 120R-100MHz-2A
C380 10uF
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Size A3
Number
Revision
Date: 8-14-2024
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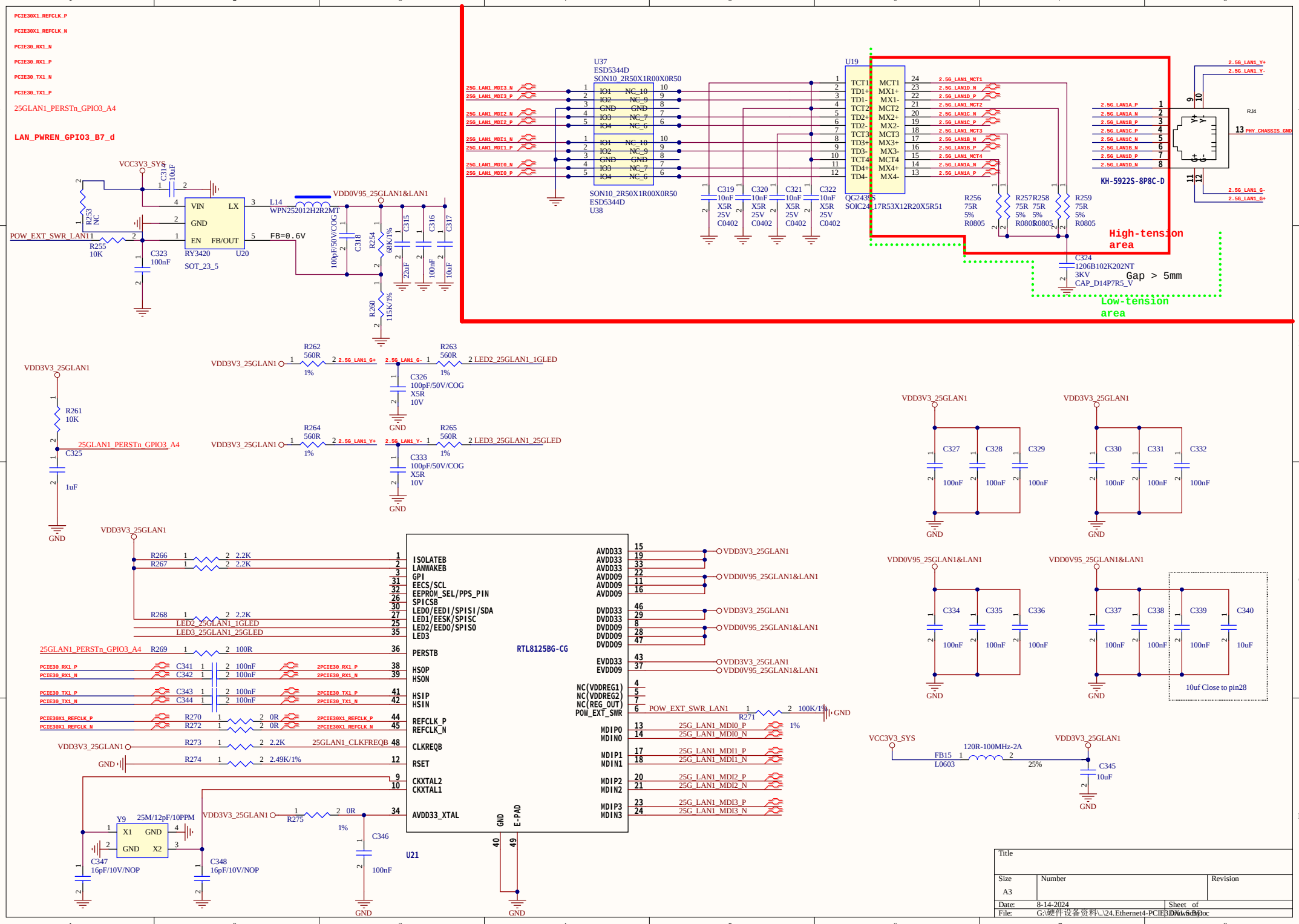

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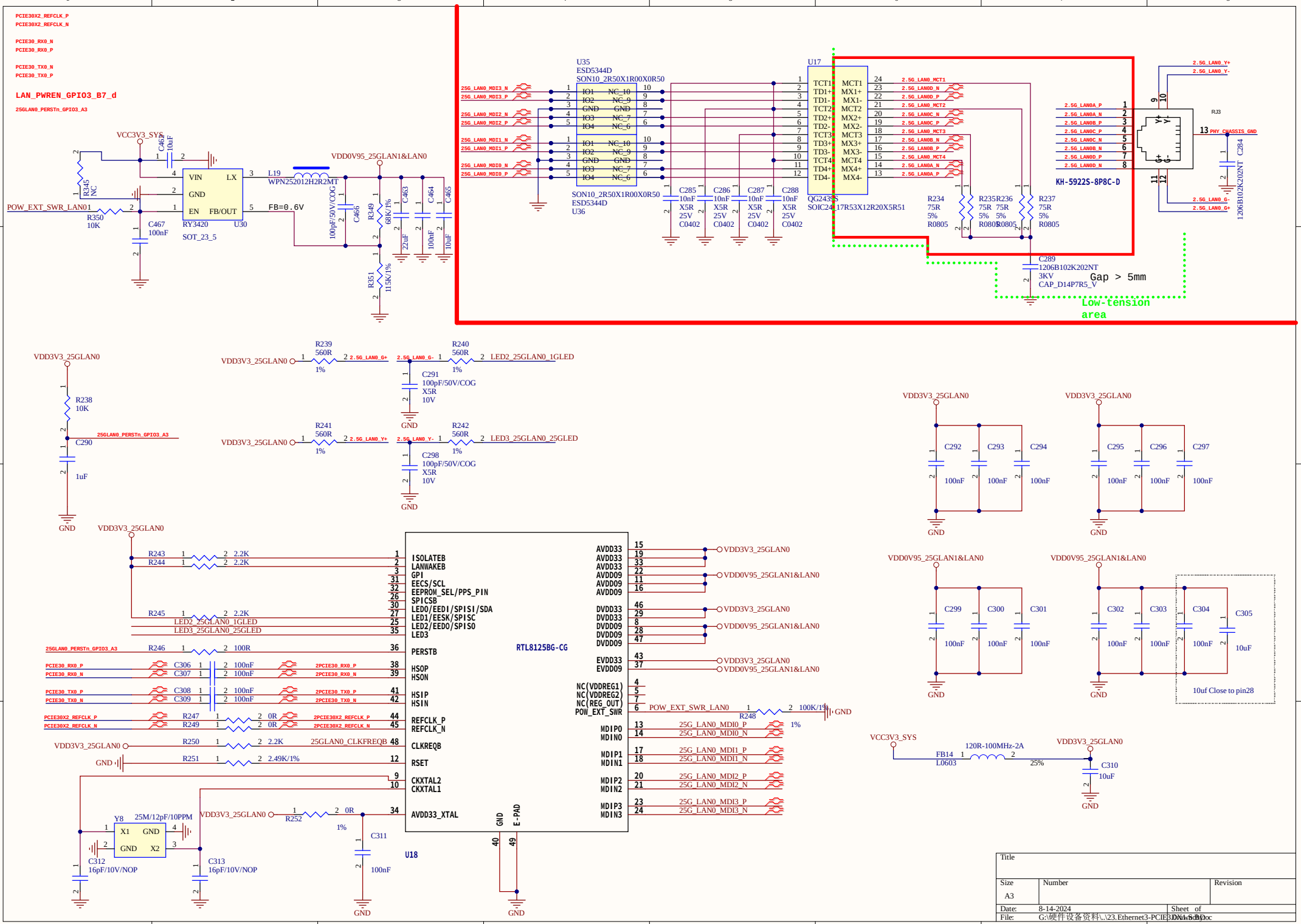
PCIE30X2_REFCLK_P
PCIE30X2_REFCLK_N
PCIE30_RX0_N
PCIE30_RX0_P
PCIE30_TX0_N
PCIE30_TX0_P
LAN_PWREN_GPIO3_B7_d
25GLAN0_PERSTn_GPIO3_A3
VCC3V3_SYS
VDD0V95_25GLAN1&LAN0
POW_EXT_SWR_LAN01
U35
ESD5344D
SON10_2R50X1R00X0R50
U36
U17
QG2435
SOIC24_17R53X12R20X5R51
KH-5922S-8P8C-D
RJ3
PHY_CHASSIS_GND
Gap > 5mm
Low-tension area
VDD3V3_25GLAN0
RTL8125BG-CG
U18
ISOLATEB
LANWAKEB
GPI
EECS/SCL
EEPROM_SEL/PPS_PIN
SPICSB
LED0/EEDI/SPISI/SDA
LED1/EESK/SPISC
LED2/EEDO/SPISO
LED3
PERSTB
HSOP
HSON
HSIP
HSIN
REFCLK_P
REFCLK_N
CLKREQB
RSET
CKXTAL2
CKXTAL1
AVDD33_XTAL
AVDD33
DVDD33
DVDD09
EVDD33
EVDD09
NC(VDDREG1)
NC(VDDREG2)
NC(REG_OUT)
POW_EXT_SWR
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
GND
E-PAD
Y8
25M/12pF/10PPM
120R-100MHz-2A
Title
Size
A3
Number
Revision
Date: 8-14-2024
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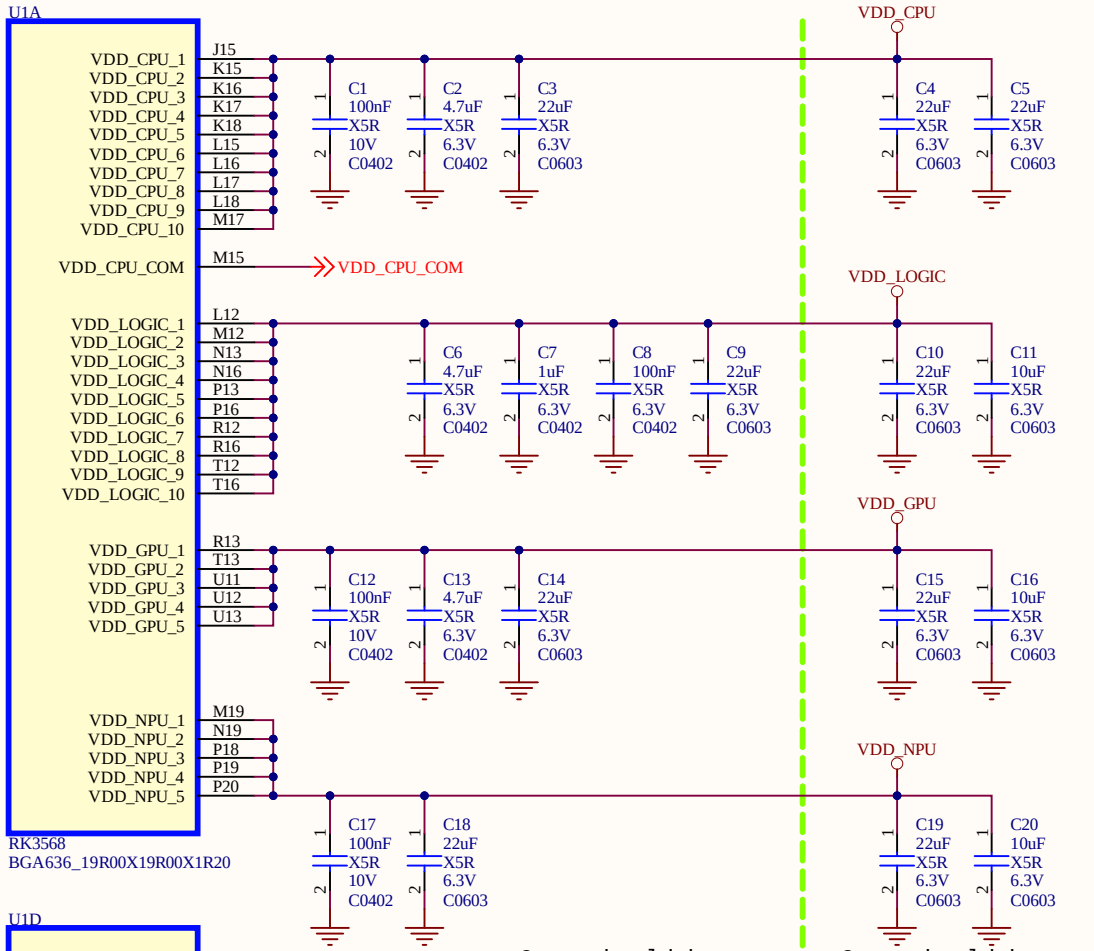
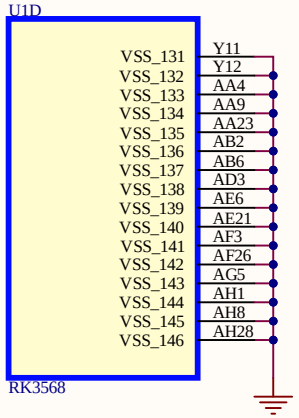
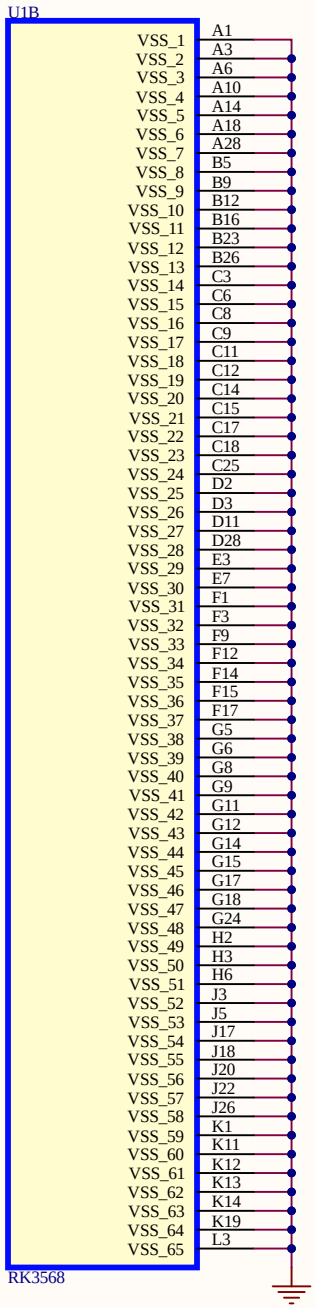
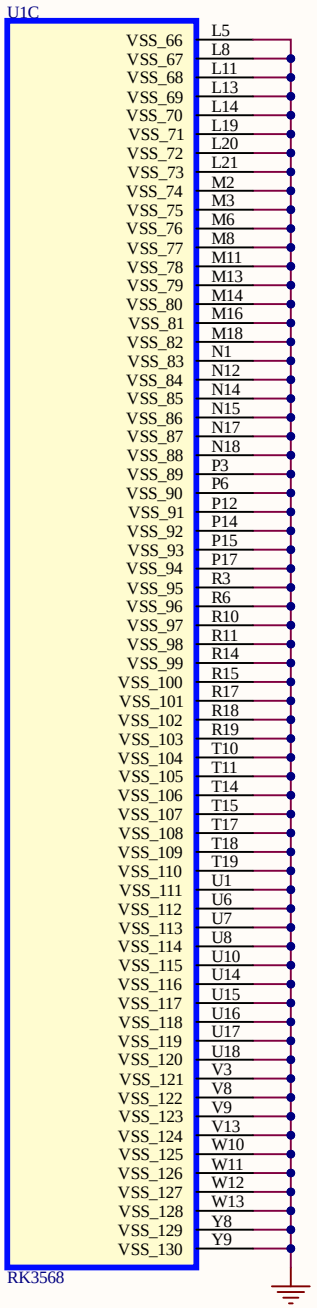
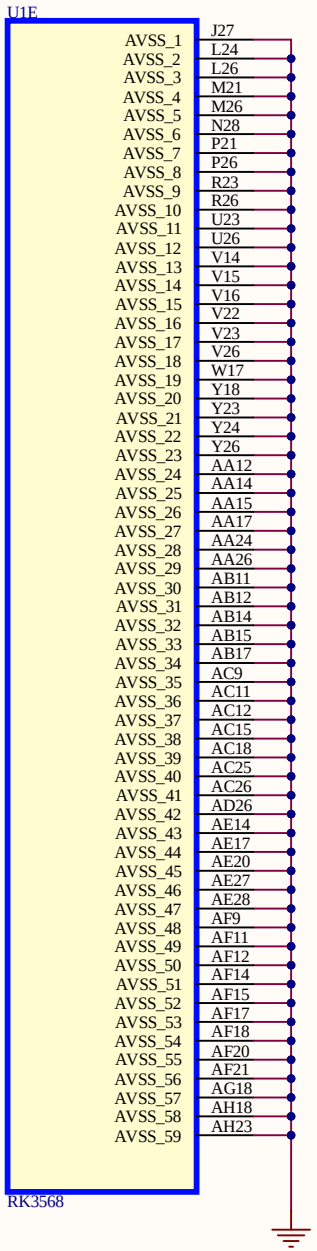
RK3568_ABCDE (Power&Gnd)



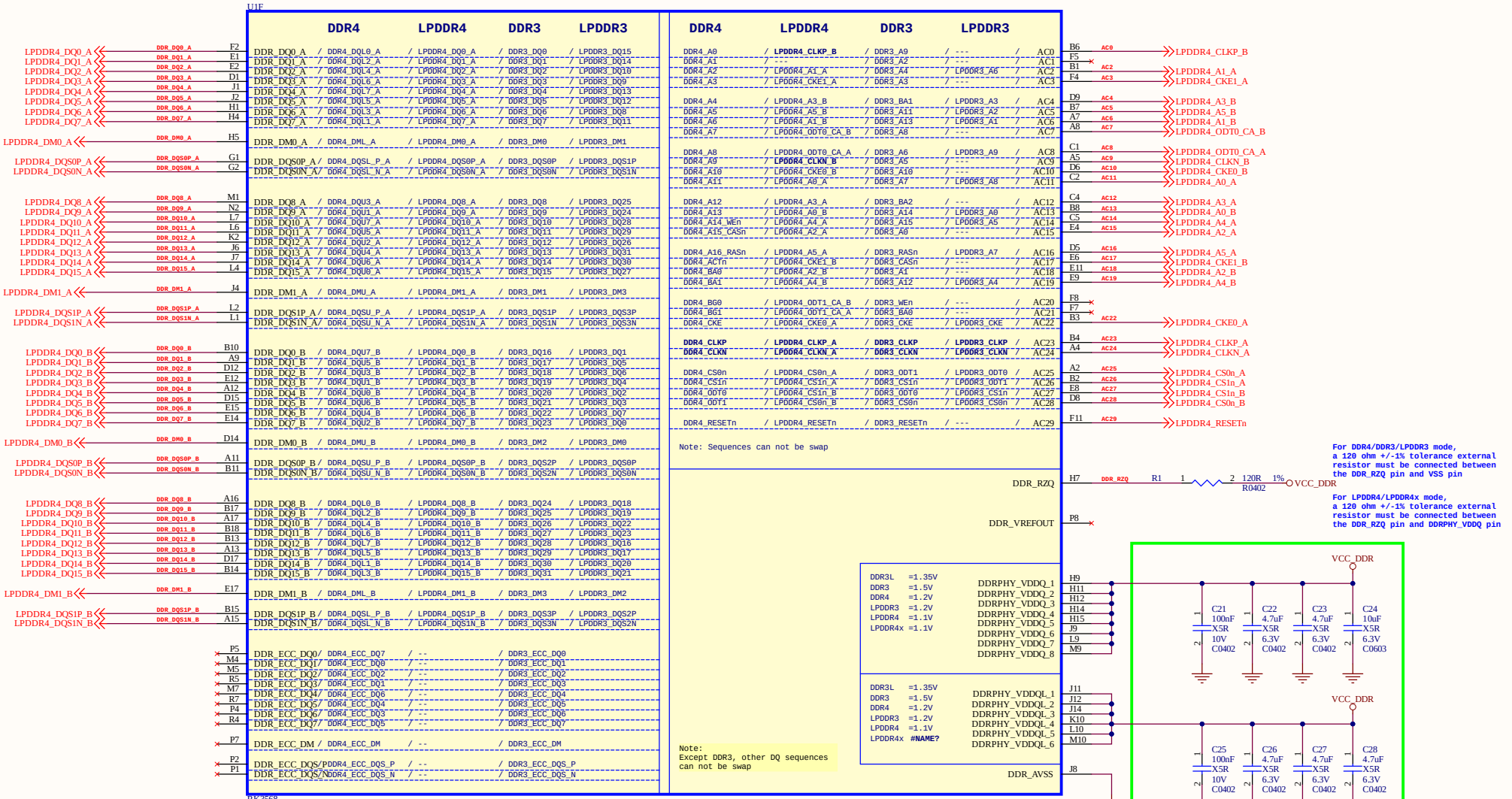








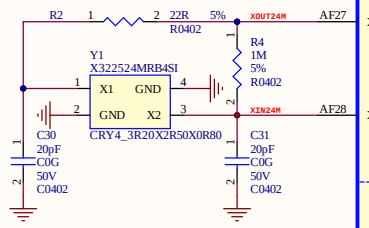
RK3568_F (DDR PHY)

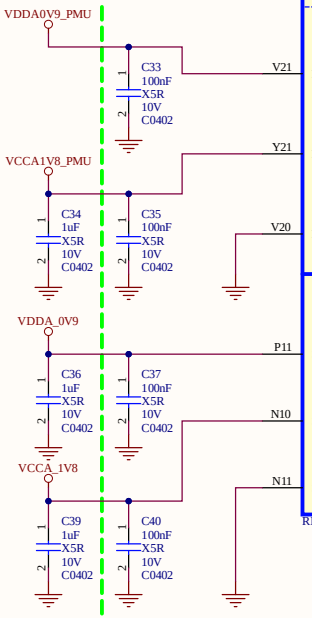


RK3568_G(OSC/PLL/PMUIO1/2)

Note:

Adjusted the load capacitance
according to the crystal specification.





U1G

OSC

XOUT24M

XIN24M

Operating Voltage
#NAME?

TVSS

GPIO0_D3_d

GPIO0_D4_d

GPIO0_D5_d

GPIO0_D6_d

PMU PLL

PMUPLL_AVDD_0V9

PMUPLL_AVDD_1V8

PMUPLL_AVSS

SYS PLL

SYSPLL_AVDD_0V9

SYSPLL_AVDD_1V8

SYSPLL_AVSS

RK3568

PMUIO1 Domain

Operating Voltage=3.3V Only

			NPOR_u	AH27
		REFCLK_OUT	GPIO0_A0_d	AG27
	TSADC_SHUT_M0	TSADC_SHUT_ORG	GPIO0_A1_z	AG26
	PMIC_SLEEP	TSADC_SHUT_M1	GPIO0_A2_d	AG28
			GPIO0_A3_u	AA22
SDMMC0_DET	SATA_CP_DET	PCIE30X1_CLKREQn_M0	GPIO0_A4_u	Y22
SDMMC0_PWREN	SATA_MP_SWITCH	PCIE20_CLKREQn_M0	GPIO0_A5_d	AF25
GPU_PWREN	SATA_CP_POD	PCIE30X2_CLKREQn_M0	GPIO0_A6_d	AE24
		FLASH_VOL_SEL	GPIO0_A7_u	AG25
			PMUIO1	Y20

PMUIO2 Domain

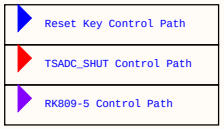
Operating Voltage=1.8V/3.3V

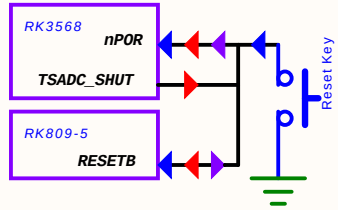
CLK32K_IN	CLK32K_OUT0	PCIE30X2_BUTTONRSTn		GPIO0_B0_u	AD23
I2C0_SCL				GPIO0_B1_u	AF24
I2C0_SDA				GPIO0_B2_u	AB21
I2C1_SCL	CAN0_TX_M0	PCIE30X1_BUTTONRSTn	MCU_JTAG_TDO	GPIO0_B3_u	AG24
I2C1_SDA	CAN0_RX_M0	PCIE20_BUTTONRSTn	MCU_JTAG_TCK	GPIO0_B4_u	AB20
I2C2_SCL_M0	SPI0_CLK_M0	PCIE20_WAKEn_M0	PWM1_M1	GPIO0_B5_u	AC22
I2C2_SDA_M0	SPI0_MOSI_M0	PCIE20_PERSTn_M0	PWM2_M1	GPIO0_B6_u	AA20
PWM0_M0	CPUAVS			GPIO0_B7_d	AH26
PWM1_M0	GPUAVS	UART0_RX		GPIO0_C0_d	AD22
PWM2_M0	NPUAVS	UART0_TX	MCU_JTAG_TDI	GPIO0_C1_d	AF23
PWM3_IR	EDP_HPDIN_M1	PCIE30X1_WAKEn_M0	MCU_JTAG_TMS	GPIO0_C2_d	AG23
PWM4	VOP_PWM_M0	PCIE30X1_PERSTn_M0	MCU_JTAG_TRSTn	GPIO0_C3_d	AE23
PWM5	SPI0_CS1_M0	UART0_RTSn		GPIO0_C4_d	AD21
PWM6	SPI0_MISO_M0	PCIE30X2_WAKEn_M0		GPIO0_C5_d	AC21
PWM7_IR	SPI0_CS0_M0	PCIE30X2_PERSTn_M0		GPIO0_C6_d	AD20
HDMITX_CEC_M1	PWM0_M1	UART0_CTSN		GPIO0_C7_d	AH25
			UART2_RX_M0	GPIO0_D0_u	AC20
			UART2_TX_M0	GPIO0_D1_u	AH24
				PMUIO2	W19

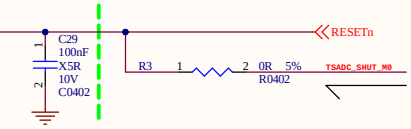
PMUIO1/2/OSC Domain Logic Power

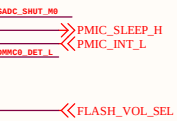
Operating Voltage=0.9V

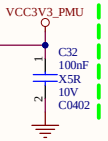
PMU_VDD_LOGIC_0V9	V19

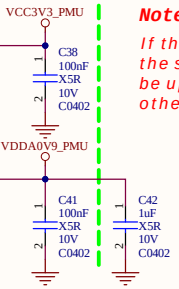




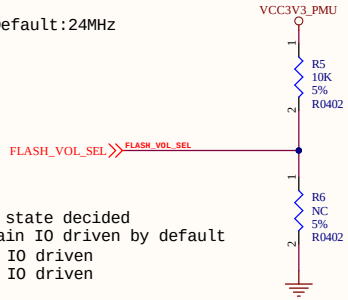




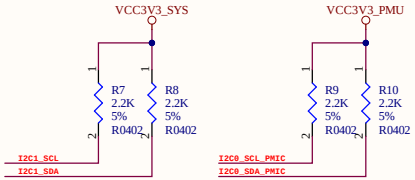




Default:24MHz



Note:
FLASH_VOL_SEL state decided
to VCCIO2 domain IO driven by default
Logic=L: 3.3V IO driven
Logic=H: 1.8V IO driven



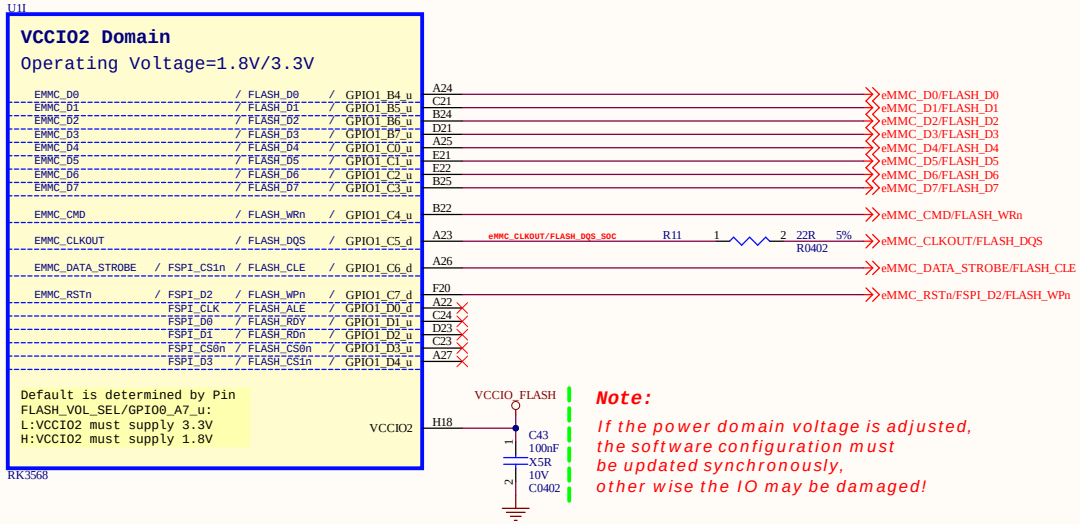
Note:

If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_I(VCCIO2 Domain)



Note:

If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

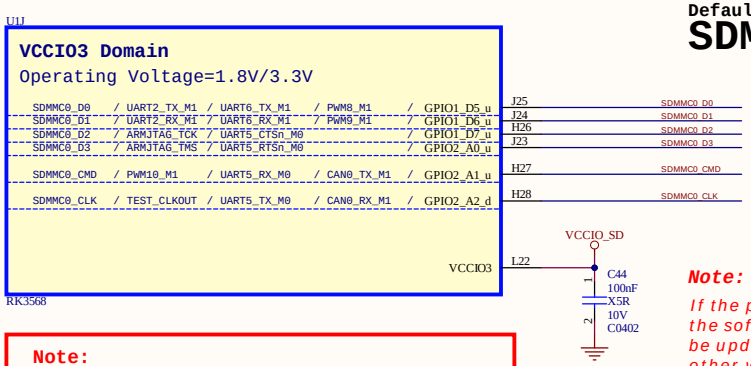
Layout note:

Test point must be placed on the line, and no branch can be added

Note:
Reserve TestPoint for put the system into Maskrom mode to update the firmware
When writing mismatched firmware or other conditions result in boot failure,
use this test point

Except in this case, please use Recovery Key
Put the system into loader mode to update the firmware

RK3568_J(VCCIO3 Domain)



Default
SDMMC0&JTAG

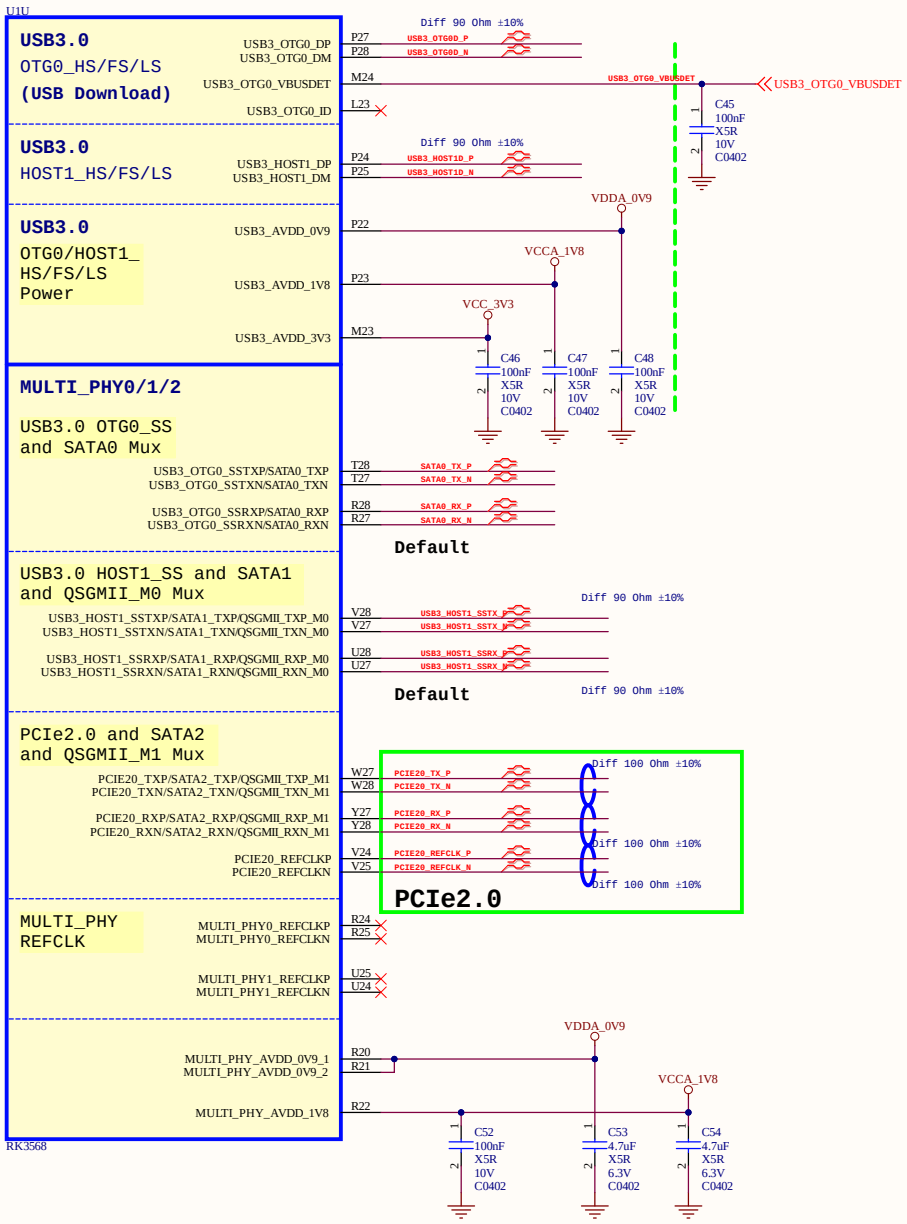
Note:

If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:

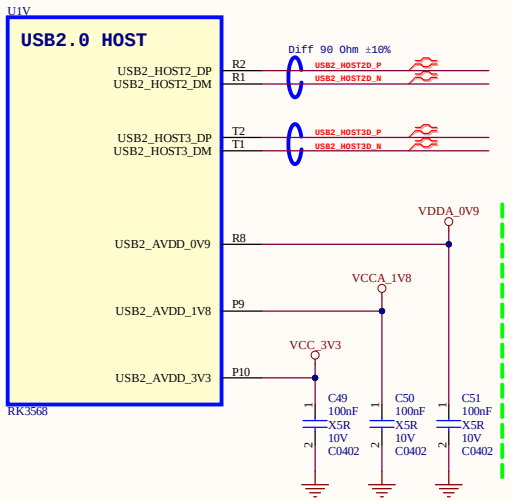
Caps of between dashed green lines and U1000
should be placed under the U1000 package

RK3568_U(USB3.0/SATA/QSGMII/PCIe2.0 x1)

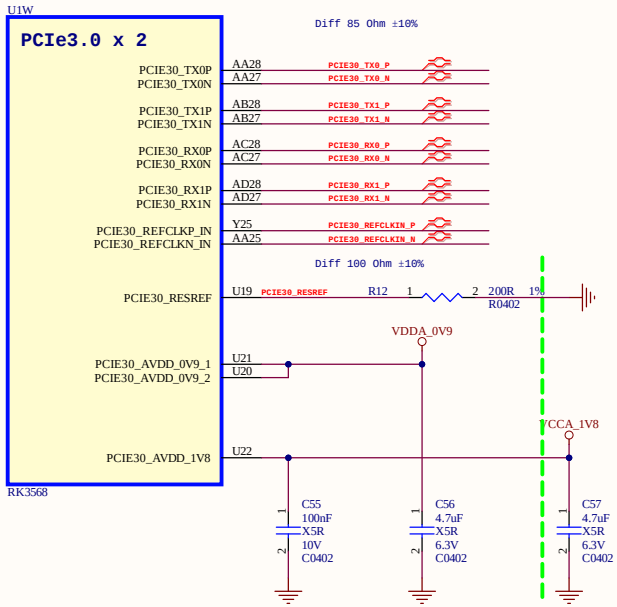


Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_V(USB2.0 HOST)



RK3568_W(PCIe3.0 x2)



RK3568_K(VCCIO4 Domain)

U1K

VCCIO4 Domain

Operating Voltage=1.8V/3.3V

SDMMC1_D0	GMAC0_RXD2	UART6_RX_M0		GPIO2_A3_u	E27 GMAC0_RXD2 → GMAC0_RXD2
SDMMC1_D1	GMAC0_RXD3	UART6_TX_M0		GPIO2_A4_u	E28 GMAC0_RXD3 → GMAC0_RXD3
SDMMC1_D2	GMAC0_RXCLK	UART7_RX_M0		GPIO2_A5_u	B28 GMAC0_RXCLK → GMAC0_RXCLK
SDMMC1_D3	GMAC0_TXD2	UART7_TX_M0		GPIO2_A6_u	C27 GMAC0_TXD2 → GMAC0_TXD2
SDMMC1_CMD	GMAC0_TXD3	UART9_RX_M0		GPIO2_A7_u	C28 GMAC0_TXD3 → GMAC0_TXD3
SDMMC1_CLK	GMAC0_TXCLK	UART9_TX_M0		GPIO2_B0_d	D27 GMAC0_TXCLK → GMAC0_TXCLK
SDMMC1_PWREN	I2C4_SDA_M1	UART8_RTSn_M0	CAN2_RX_M1	GPIO2_B1_d	D26 → UART8_RTSn_M0
SDMMC1_DET	I2C4_SCL_M1	UART8_CTSn_M0	CAN2_TX_M1	GPIO2_B2_u	E25 → UART8_CTSn_M0
	GMAC0_TXD0	UART1_RX_M0		GPIO2_B3_u	F28 GMAC0_TXD0 → GMAC0_TXD0
	GMAC0_TXD1	UART1_TX_M0		GPIO2_B4_u	G27 GMAC0_TXD1 → GMAC0_TXD1
	GMAC0_TXEN	UART1_RTSn_M0	SPI1_CLK_M0	GPIO2_B5_u	G28 GMAC0_TXEN → GMAC0_TXEN
	GMAC0_RXD0	UART1_CTSn_M0	SPI1_MISO_M0	GPIO2_B6_u	F27 GMAC0_RXD0 → GMAC0_RXD0
I2S2_SCLK_RX_M0	GMAC0_RXD1	UART6_RTSn_M0	SPI1_MOSI_M0	GPIO2_B7_d	H25 GMAC0_RXD1 → GMAC0_RXD1
I2S2_LRCK_RX_M0	GMAC0_RXDV_CRS	UART6_CTSn_M0	SPI1_CS0_M0	GPIO2_C0_d	F24 GMAC0_RXDV_CRS → GMAC0_RXDV_CRS
I2S2_MCLK_M0	ETH0_REFCLKO_25M	UART7_RTSn_M0	SPI2_CLK_M0	GPIO2_C1_d	G23
I2S2_SCLK_TX_M0	GMAC0_MCLKINOUT	UART7_CTSn_M0	SPI2_MISO_M0	GPIO2_C2_d	F25 GMAC0_MCLKINOUT → GMAC0_MCLKINOUT
I2S2_LRCK_TX_M0	GMAC0_MDC	UART9_RTSn_M0	SPI2_MOSI_M0	GPIO2_C3_d	H24 GMAC0_MDC → GMAC0_MDC
I2S2_SDO_M0	GMAC0_MDIO	UART9_CTSn_M0	SPI2_CS0_M0	GPIO2_C4_d	H23 GMAC0_MDIO → GMAC0_MDIO
I2S2_SDI_M0	GMAC0_RXER	UART8_TX_M0	SPI2_CS1_M0	GPIO2_C5_d	F26 → UART8_TX_M0
CLK32K_OUT1		UART8_RX_M0	SPI1_CS1_M0	GPIO2_C6_d	E26 → UART8_RX_M0
				VCCIO4	

RK3568

VCCIO4 — J21 — C58 100nF X5R 10V C0402

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

VCCIO4 — R13 1 2 0R 5% R0402 — VCC_1V8

R14 1 2 NC 5% R0402 — VCC_3V3

Note:

According to the actual choice of mounted
Cannot be mounted at the same time

Default:1.8V

Select the voltage according to the application

RGMII0+UART8

Note:

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

If Ethernet PHY uses other models, please note whether the default pull-up and pull-down of GPIO affect Ethernet PHY function

At present, TXEN will be affected if it defaults to high level need to add a 4.7K resistance to ground

RK3568_N(VCCIO7 Domain)

U1N

VCCIO7 Domain

Operating Voltage=1.8V/3.3V

PWM14_M1	SPI3_CLK_M1	CAN1_RX_M1	PCIE30X2_CLKREQn_M2	GPIO4_C2_d	AF8 GPIO4_C2
PWM15_IR_M1	SPI3_MOSI_M1	CAN1_TX_M1	PCIE30X2_WAKEn_M2	GPIO4_C3_d	AA11 GPIO4_C3
EDP_HPDIN_M0	SPDIF_TX_M2	SATA2_ACT_LED	PCIE30X2_PERSTn_M2	GPIO4_C4_d	AH7 GPIO4_C4 → GPIO4_C4
PWM12_M1	SPI3_MISO_M1	SATA1_ACT_LED	UART9_TX_M1	GPIO4_C5_d	AD8 GPIO4_C5
PWM13_M1	SPI3_CS0_M1	SATA0_ACT_LED	UART9_RX_M1	GPIO4_C6_d	AE8 GPIO4_C6
HDMITX_SCL	I2C5_SCL_M1			GPIO4_C7_u	AG8 → HDMITX_SCL
HDMITX_SDA	I2C5_SDA_M1			GPIO4_D0_u	AG7 → HDMITX_SDA
HDMITX_CEC_M0	SPI3_CS1_M1			GPIO4_D1_u	AH6 → HDMITX_CEC_M0
				GPIO4_D2_d	AB9
				VCCIO7	V12

RK3568

VCC_3V3 — C61 100nF X5R 10V C0402

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Default

GPIO4_C5 GPIO4_C6 → UART9_TX_M1 UART9_RX_M1

Option

GPIO4_C5 GPIO4_C6 → SATA1_ACT_LED SATA0_ACT_LED

RK3568_O(SARADC/OTP)

U1O

SARADC

Recovery	SARADC_VIN0	B27	SARADC_VIN0_KEY/RECOVERY
	SARADC_VIN1	C26	SARADC_VIN1_HW_ID
	SARADC_VIN2	D24	
	SARADC_VIN3	E23	
	SARADC_VIN4	G21	
	SARADC_VIN5	F22	
	SARADC_VIN6	G20	
	SARADC_VIN7	F21	
	SARADC_AVDD_1V8	H22	

OTP

	OTP_VCC18	H20

RK3568

SARADC_VIN0_KEY/RECOVERY — C59 1 2 1nF X5R 50V C0402

SARADC_VIN1_HW_ID — C60 1 2 1nF X5R 50V C0402

R16 1 2 22R RECOVERY R0402 5% — SW1 — GND

VCCA_1V8 — C62 100nF X5R 10V C0402

VCC_1V8 — C63 100nF X5R 10V C0402

VCCA_1V8 — R17 10K 1% R0402 — SARADC_VIN1_HW_ID

R18 10K 1% R0402

Note:

Must be mounted

VCCA_1V8 — R15 10K 1% R0402 — SARADC_VIN0_KEY/RECOVERY

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

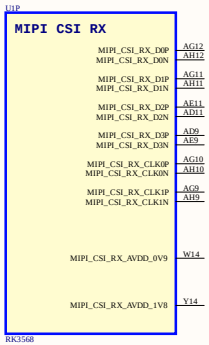
Note:

If there is no Key requirement, two test points must be reserved to facilitate firmware update

It is suggested to reserve a Key to facilitate the development debug

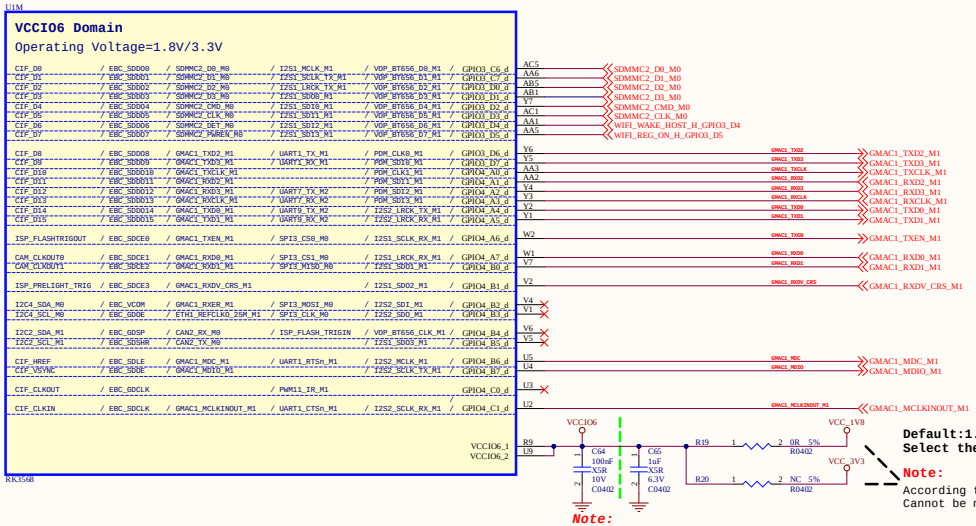
If SARADC_VIN0=0V at after power on and reset, then system will enter into loader mode.

RK3568_P(MIPI_CSI_RX)



Option1	Sensor1 x4Lane	MIPI_CSI_RX_D0-3 MIPI_CSI_RX_CLK0
Option2	Sensor1 x2Lane + Sensor2 x2Lane	MIPI_CSI_RX_D0-1 MIPI_CSI_RX_CLK0 MIPI_CSI_RX_D2-3 MIPI_CSI_RX_CLK1

RK3568_M(VCCIO6 Domain)



Default:1.8V
Select the voltage according to the application

Note:
According to the actual choice of mounted
Cannot be mounted at the same time

Note:
If the power domain voltage is adjusted,
the software configuration must
be updated synchronously,
other wise the IO may be damaged!

Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

Note:
Camera MCLK can select the following clock:
1:CAM_CLKOUT0
2:CAM_CLKOUT1
3:CIF_CLKOUT
4:REFCLK_OUT

Attention to the voltage matching

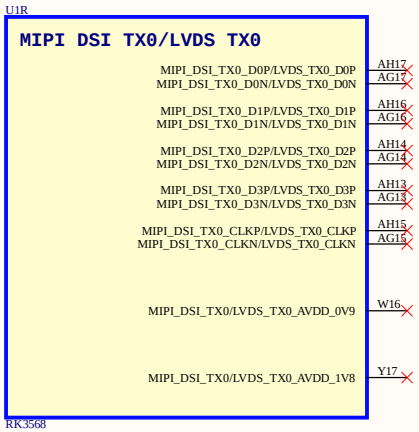
Mode	16bit	12bit	10bit	8bit
CIF_D0	D0	--	--	--
CIF_D1	D1	--	--	--
CIF_D2	D2	--	--	--
CIF_D3	D3	--	--	--
CIF_D4	D4	D0	--	--
CIF_D5	D5	D1	--	--
CIF_D6	D6	D2	D0	--
CIF_D7	D7	D3	D1	--
CIF_D8	D8	D4	D2	D0
CIF_D9	D9	D5	D3	D1
CIF_D10	D10	D6	D4	D2
CIF_D11	D11	D7	D5	D3
CIF_D12	D12	D8	D6	D4
CIF_D13	D13	D9	D7	D5
CIF_D14	D14	D10	D8	D6
CIF_D15	D15	D11	D9	D7

Support BT601 YCbCr 422 8bit input
Support BT656 YCbCr 422 8bit input
Support RAW 8/10/12bit input
Support BT1120 YCbCr 422 8/10/12/16bit input, single/dual-edge sampling
Support 2/4 mixed BT656/BT1120 YCbCr 422 8bit input

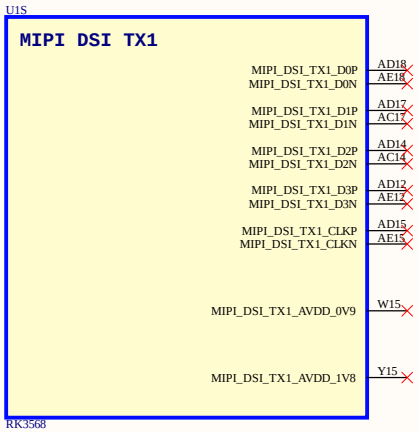
BT1120 16bit Mode:
Default: D0-D7 <--> Y0-Y7 , D8-D15 <--> C0-C7
Swap ON: D0-D7 <--> C0-C7 , D8-D15 <--> Y0-Y7

GMAC	Direction	GEPHY	GMAC	Direction	FEPHY
GMACx_TXD0	------>	PHYx_TXD0	GMACx_TXD0	------>	PHYx_TXD0
GMACx_TXD1	------>	PHYx_TXD1	GMACx_TXD1	------>	PHYx_TXD1
GMACx_TXD2	------>	PHYx_TXD2			
GMACx_TXD3	------>	PHYx_TXD3			
GMACx_TXEN	------>	PHYx_TXEN	GMACx_TXEN	------>	PHYx_TXEN
GMACx_TXCLK	------>	PHYx_TXCLK			
GMACx_RXD0	<------	PHYx_RXD0	GMACx_RXD0	<------	PHYx_RXD0
GMACx_RXD1	<------	PHYx_RXD1	GMACx_RXD1	<------	PHYx_RXD1
GMACx_RXD2	<------	PHYx_RXD2			
GMACx_RXD3	<------	PHYx_RXD3			
GMACx_RXDV	<------	PHYx_RXDV	GMACx_RXDV	<------	PHYx_RXDV
GMACx_RXCLK	<------	PHYx_RXCLK			
GMACx_RXER			GMACx_RXER	<------	PHYx_RXER
GMACx_MDC	------>	PHYx_MDC	GMACx_MDC	------>	PHYx_MDC
GMACx_MDIO	<------>	PHYx_MDIO	GMACx_MDIO	<------>	PHYx_MDIO
ETHx_REFCLKO_25M	------>	PHYx_XTALIN			
GMACx_MCLKINOUT	<------	PHYx_CLKOUT125(Option)	GMACx_MCLKINOUT	------>	PHYx_XTALIN/REFCLK
GPIO	------>	PHYx_RSTn	GPIO	------>	PHYx_RSTn
GPIO	<------	PHYx_INT/PMEB	GPIO	<------	PHYx_INT/PMEB

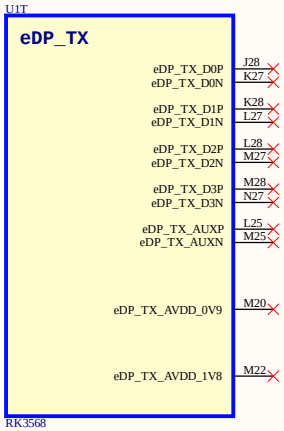
RK3568_R(MIPI_DSI_TX0/LVDS_TX0)



RK3568_S(MIPI_DSI_TX1)

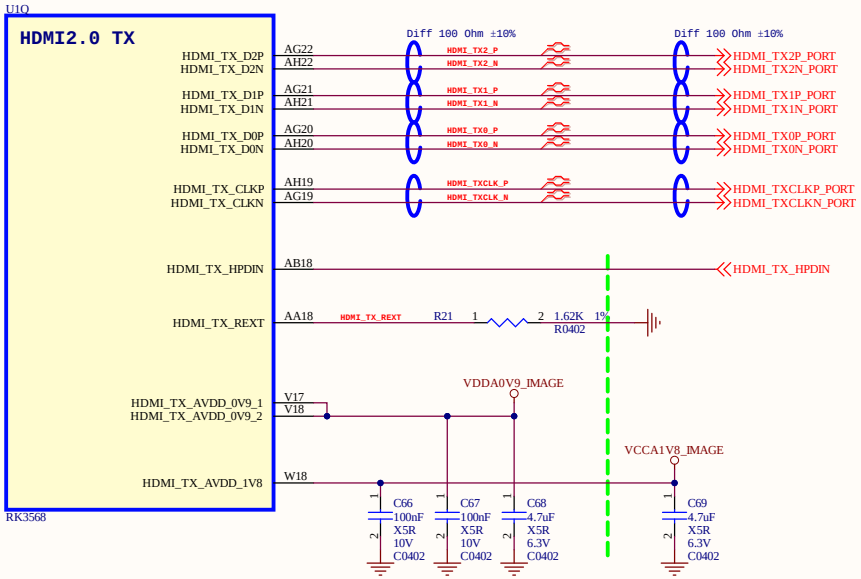


RK3568_T(eDP TX)



Note:
Caps of between dashed green lines and U1000
should be placed under the U1000 package.
Other caps should be placed close to the U1000 package

RK3568_Q(HDMI2.0 TX)



RK3568_L(VCCIO5 Domain)

U1L

VCCIO5 Domain

Operating Voltage=1.8V/3.3V

LCDC_D0	VOP_BT656_D0_M0	SPI0_MISO_M1	PCIE20_CLKREQn_M1	I2S1_MCLK_M2	GPIO2_D0_d	AG6
LCDC_D1	VOP_BT656_D1_M0	SPI0_MOSI_M1	PCIE20_WAKEn_M1	I2S1_SCLK_TX_M2	GPIO2_D1_d	AD7
LCDC_D2	VOP_BT656_D2_M0	SPI0_CS0_M1	PCIE30X1_CLKREQn_M1	I2S1_LRCK_TX_M2	GPIO2_D2_d	AC8
LCDC_D3	VOP_BT656_D3_M0	SPI0_CLK_M1	PCIE30X1_WAKEn_M1	I2S1_SDI0_M2	GPIO2_D3_d	AC7
LCDC_D4	VOP_BT656_D4_M0	SPI2_CS1_M1	PCIE30X2_CLKREQn_M1	I2S1_SDI1_M2	GPIO2_D4_d	AF5
LCDC_D5	VOP_BT656_D5_M0	SPI2_CS0_M1	PCIE30X2_WAKEn_M1	I2S1_SDI2_M2	GPIO2_D5_d	AF6
LCDC_D6	VOP_BT656_D6_M0	SPI2_MOSI_M1	PCIE30X2_PERSTn_M1	I2S1_SDI3_M2	GPIO2_D6_d	AD6
LCDC_D7	VOP_BT656_D7_M0	SPI2_MISO_M1	UART8_TX_M1	I2S1_SDO0_M2	GPIO2_D7_d	AH5
LCDC_CLK	VOP_BT656_CLK_M0	SPI2_CLK_M1	UART8_RX_M1	I2S1_SDO1_M2	GPIO3_A0_d	AH4
LCDC_D8	VOP_BT1120_D0	SPI1_CS0_M1	PCIE30X1_PERSTn_M1	SDMMC2_D0_M1	GPIO3_A1_d	AB8
LCDC_D9	VOP_BT1120_D1	GMAC1_TXD2_M0	I2S3_MCLK_M0	SDMMC2_D1_M1	GPIO3_A2_d	AE5
LCDC_D10	VOP_BT1120_D2	GMAC1_TXD3_M0	I2S3_SCLK_M0	SDMMC2_D2_M1	GPIO3_A3_d	AG4
LCDC_D11	VOP_BT1120_D3	GMAC1_RXD2_M0	I2S3_LRCK_M0	SDMMC2_D3_M1	GPIO3_A4_d	AF4
LCDC_D12	VOP_BT1120_D4	GMAC1_RXD3_M0	I2S3_SDO_M0	SDMMC2_CMD_M1	GPIO3_A5_d	AH3
LCDC_D13	VOP_BT1120_CLK	GMAC1_TXCLK_M0	I2S3_SDI_M0	SDMMC2_CLK_M1	GPIO3_A6_d	AG3
LCDC_D14	VOP_BT1120_D5	GMAC1_RXCLK_M0		SDMMC2_DET_M1	GPIO3_A7_d	AH2
LCDC_D15	VOP_BT1120_D6	ETH1_REFCLKO_25M_M0		SDMMC2_PWREN_M1	GPIO3_B0_d	AG2
LCDC_D16	VOP_BT1120_D7	GMAC1_RXD0_M0	UART4_RX_M1	PWM8_M0	GPIO3_B1_d	AG1
LCDC_D17	VOP_BT1120_D8	GMAC1_RXD1_M0	UART4_TX_M1	PWM9_M0	GPIO3_B2_d	AF2
LCDC_D18	VOP_BT1120_D9	GMAC1_RXDV_CRS_M0	I2C5_SCL_M0	PDM_SDI0_M2	GPIO3_B3_d	AF1
LCDC_D19	VOP_BT1120_D10	GMAC1_RXER_M0	I2C5_SDA_M0	PDM_SDI1_M2	GPIO3_B4_d	AE1
LCDC_D20	VOP_BT1120_D11	GMAC1_TXD0_M0	I2C3_SCL_M1	PWM10_M0	GPIO3_B5_d	AE2
LCDC_D21	VOP_BT1120_D12	GMAC1_TXD1_M0	I2C3_SDA_M1	PWM11_IR_M0	GPIO3_B6_d	AE3
LCDC_D22	PWM12_M0	GMAC1_TXEN_M0	UART3_TX_M1	PDM_SDI2_M2	GPIO3_B7_d	AD4
LCDC_D23	PWM13_M0	GMAC1_MCLKINOUT_M0	UART3_RX_M1	PDM_SDI3_M2	GPIO3_C0_d	AD2
LCDC_HSYNC	VOP_BT1120_D13	SPI1_MOSI_M1	PCIE20_PERSTn_M1	I2S1_SDO2_M2	GPIO3_C1_d	AD1
LCDC_VSYNC	VOP_BT1120_D14	SPI1_MISO_M1	UART5_TX_M1	I2S1_SDO3_M2	GPIO3_C2_d	AA7
LCDC_DEN	VOP_BT1120_D15	SPI1_CLK_M1	UART5_RX_M1	I2S1_SCLK_RX_M2	GPIO3_C3_d	AC4
PWM14_M0	VOP_PWM_M1	GMAC1_MDC_M0	UART7_TX_M1	PDM_CLK1_M2	GPIO3_C4_d	AC3
PWM15_IR_M0	SPDIF_TX_M1	GMAC1_MDIO_M0	UART7_RX_M1	I2S1_LRCK_RX_M2	GPIO3_C5_d	AC2

VCCIO5_1 V10
VCCIO5_2 V11

RK3568

PCIE20_CLKREQn_M1
PCIE20_WAKEn_M1
GMAC0_INT/PMEB_GPIO2_D2
GMAC0_RSTN_GPIO2_D3
GMAC1_INT/PMEB_GPIO2_D4
GMAC1_RSTN_GPIO2_D5
GPIO2_D7
25GLAN0_PERSTn_GPIO3_A3
25GLAN1_PERSTn_GPIO3_A4
25GLAN2_PERSTn_GPIO3_A5
I2C5_SCL_M0
I2C5_SDA_M0
I2C3_SCL_M1
I2C3_SDA_M1
LAN_PWREN_GPIO3_B7_d
PCIE20_PERSTn_M1
UART5_TX_M1
UART5_RX_M1
UART7_TX_M1
UART7_RX_M1

VCC_3V3

R22 2.2K 5% R0402
R23 2.2K 5% R0402
R24 2.2K 5% R0402
R25 2.2K 5% R0402

C70 100nF X5R 10V C0402

Note:

If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

Note:

Caps of between dashed green lines and U1000 should be placed under the U1000 package

RK3568_H(VCCIO1 Domain)

U1H

VCCIO1 Domain

Operating Voltage=1.8V/3.3V

I2C3_SDA_M0	/ UART3_RX_M0	/ CAN1_RX_M0	/ AUDIOPWM_LOUT_P	/ ACODEC_ADC_DATA	/ GPIO1_A0_u	D18	
I2C3_SCL_M0	/ UART3_TX_M0	/ CAN1_TX_M0	/ AUDIOPWM_LOUT_N	/ ACODEC_ADC_CLK	/ GPIO1_A1_u	E18	
I2S1_MCLK_M0	/ UART3_RTSn_M0	/ SCR_CLK	/ PCIE30X1_PERSTn_M2		/ GPIO1_A2_d	A19	I2S1_MCLK_M0_RK809
I2S1_SCLK_TX_M0	/ UART3_CTSn_M0	/ SCR_IO	/ PCIE30X1_WAKEn_M2	/ ACODEC_DAC_CLK	/ GPIO1_A3_d	B19	I2S1_SCLK_TX_M0_RK809
I2S1_SCLK_RX_M0	/ UART4_RX_M0	/ PDM_CLK1_M0	/ SPDIF_TX_M0		/ GPIO1_A4_d	F18	
I2S1_LRCK_TX_M0	/ UART4_RTSn_M0	/ SCR_RST	/ PCIE30X1_CLKREQn_M2	/ ACODEC_DAC_SYNC	/ GPIO1_A5_d	A20	I2S1_LRCK_TX_M0_RK809
I2S1_LRCK_RX_M0	/ UART4_TX_M0	/ PDM_CLK0_M0	/ AUDIOPWM_ROUT_P		/ GPIO1_A6_d	C20	PDM_CLK0_M0_RK809
I2S1_SDO0_M0	/ UART4_CTSn_M0	/ SCR_DET	/ AUDIOPWM_ROUT_N	/ ACODEC_DAC_DATAL	/ GPIO1_A7_d	B20	I2S1_SDO0_M0_RK809
I2S1_SDO1_M0	/ I2S1_SDI3_M0	/ PDM_SDI3_M0	/ PCIE20_CLKREQn_M2	/ ACODEC_DAC_DATAR	/ GPIO1_B0_d	D20	
I2S1_SDO2_M0	/ I2S1_SDI2_M0	/ PDM_SDI2_M0	/ PCIE20_WAKEn_M2	/ ACODEC_ADC_SYNC	/ GPIO1_B1_d	E20	
I2S1_SDO3_M0	/ I2S1_SDI1_M0	/ PDM_SDI1_M0	/ PCIE20_PERSTn_M2		/ GPIO1_B2_d	A21	
	I2S1_SDI0_M0	/ PDM_SDI0_M0			/ GPIO1_B3_d	B21	I2S1_SDI0_M0/PDM_SDI0_M0_RK809

VCCIO1 H17

VCCIO_ACODEC

C71 100nF X5R 10V C0402

Default 3.3V

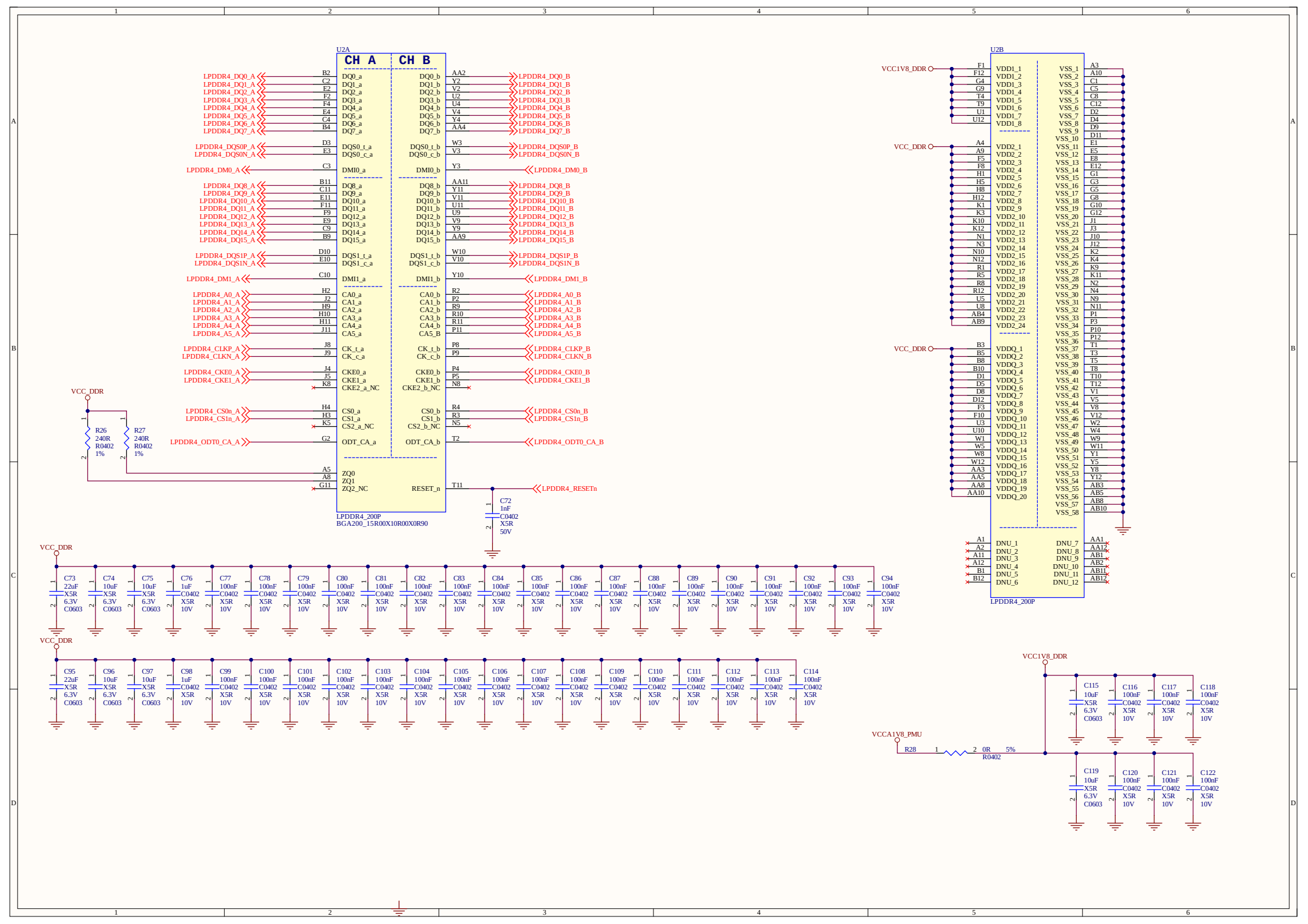
Note:

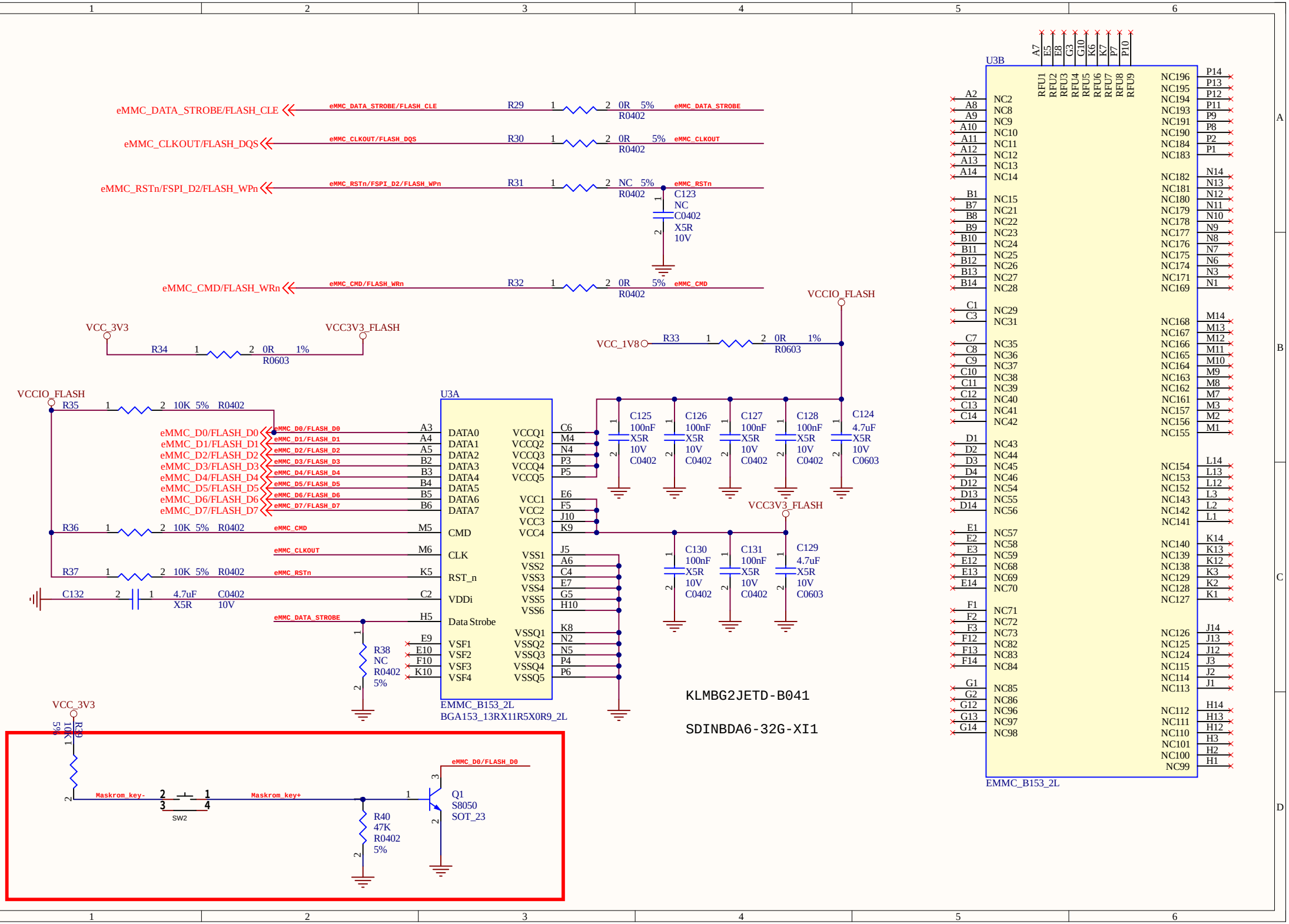
If the power domain voltage is adjusted, the software configuration must be updated synchronously, other wise the IO may be damaged!

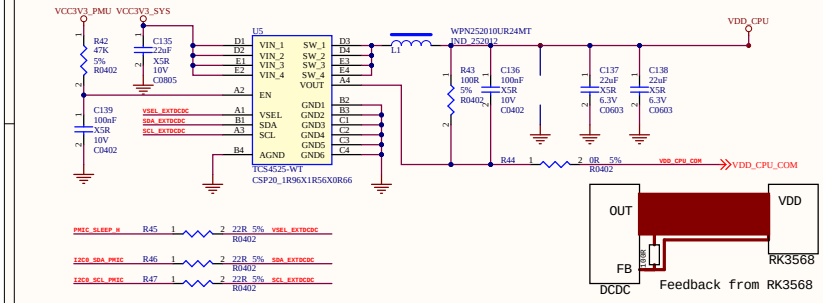
RK3568

Note:

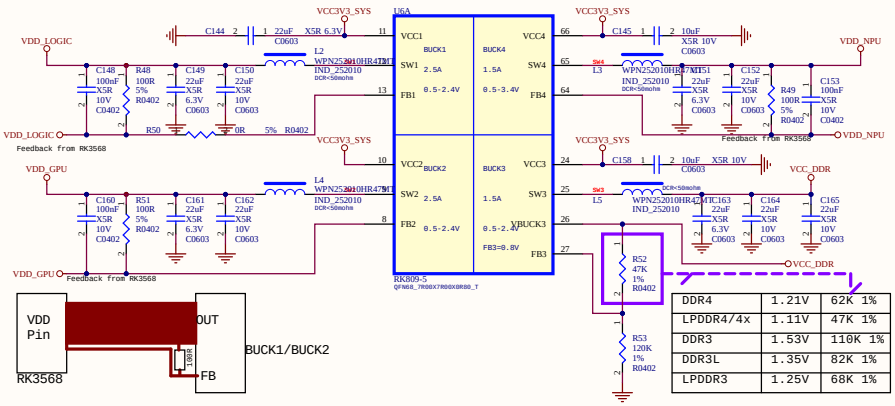
Caps of between dashed green lines and U1000 should be placed under the U1000 package


U2A
CH A
CH B
LPDDR4_DQ0_A
LPDDR4_DQ1_A
LPDDR4_DQ2_A
LPDDR4_DQ3_A
LPDDR4_DQ4_A
LPDDR4_DQ5_A
LPDDR4_DQ6_A
LPDDR4_DQ7_A
LPDDR4_DQS0P_A
LPDDR4_DQS0N_A
LPDDR4_DM0_A
LPDDR4_DQ8_A
LPDDR4_DQ9_A
LPDDR4_DQ10_A
LPDDR4_DQ11_A
LPDDR4_DQ12_A
LPDDR4_DQ13_A
LPDDR4_DQ14_A
LPDDR4_DQ15_A
LPDDR4_DQS1P_A
LPDDR4_DQS1N_A
LPDDR4_DM1_A
LPDDR4_A0_A
LPDDR4_A1_A
LPDDR4_A2_A
LPDDR4_A3_A
LPDDR4_A4_A
LPDDR4_A5_A
LPDDR4_CLKP_A
LPDDR4_CLKN_A
LPDDR4_CKE0_A
LPDDR4_CKE1_A
LPDDR4_CS0n_A
LPDDR4_CS1n_A
LPDDR4_ODT0_CA_A
LPDDR4_DQ0_B
LPDDR4_DQ1_B
LPDDR4_DQ2_B
LPDDR4_DQ3_B
LPDDR4_DQ4_B
LPDDR4_DQ5_B
LPDDR4_DQ6_B
LPDDR4_DQ7_B
LPDDR4_DQS0P_B
LPDDR4_DQS0N_B
LPDDR4_DM0_B
LPDDR4_DQ8_B
LPDDR4_DQ9_B
LPDDR4_DQ10_B
LPDDR4_DQ11_B
LPDDR4_DQ12_B
LPDDR4_DQ13_B
LPDDR4_DQ14_B
LPDDR4_DQ15_B
LPDDR4_DQS1P_B
LPDDR4_DQS1N_B
LPDDR4_DM1_B
LPDDR4_A0_B
LPDDR4_A1_B
LPDDR4_A2_B
LPDDR4_A3_B
LPDDR4_A4_B
LPDDR4_A5_B
LPDDR4_CLKP_B
LPDDR4_CLKN_B
LPDDR4_CKE0_B
LPDDR4_CKE1_B
LPDDR4_CS0n_B
LPDDR4_CS1n_B
LPDDR4_ODT0_CA_B
LPDDR4_RESETn
VCC_DDR
R26 240R R0402 1%
R27 240R R0402 1%
C72 1nF C0402 X5R 50V
LPDDR4_200P
BGA200_15R00X10R00X0R90
U2B
VCC1V8_DDR
VCC_DDR
LPDDR4_200P
C73 22uF X5R 6.3V C0603
C74 10uF X5R 6.3V C0603
C75 10uF X5R 6.3V C0603
C76 1uF C0402 X5R 10V
C77 100nF C0402 X5R 10V
C78 100nF C0402 X5R 10V
C79 100nF C0402 X5R 10V
C80 100nF C0402 X5R 10V
C81 100nF C0402 X5R 10V
C82 100nF C0402 X5R 10V
C83 100nF C0402 X5R 10V
C84 100nF C0402 X5R 10V
C85 100nF C0402 X5R 10V
C86 100nF C0402 X5R 10V
C87 100nF C0402 X5R 10V
C88 100nF C0402 X5R 10V
C89 100nF C0402 X5R 10V
C90 100nF C0402 X5R 10V
C91 100nF C0402 X5R 10V
C92 100nF C0402 X5R 10V
C93 100nF C0402 X5R 10V
C94 100nF C0402 X5R 10V
C95 22uF X5R 6.3V C0603
C96 10uF X5R 6.3V C0603
C97 10uF X5R 6.3V C0603
C98 1uF C0402 X5R 10V
C99 100nF C0402 X5R 10V
C100 100nF C0402 X5R 10V
C101 100nF C0402 X5R 10V
C102 100nF C0402 X5R 10V
C103 100nF C0402 X5R 10V
C104 100nF C0402 X5R 10V
C105 100nF C0402 X5R 10V
C106 100nF C0402 X5R 10V
C107 100nF C0402 X5R 10V
C108 100nF C0402 X5R 10V
C109 100nF C0402 X5R 10V
C110 100nF C0402 X5R 10V
C111 100nF C0402 X5R 10V
C112 100nF C0402 X5R 10V
C113 100nF C0402 X5R 10V
C114 100nF C0402 X5R 10V
VCC1V8_DDR
VCCA1V8_PMU
R28 0R 5% R0402
C115 10uF X5R 6.3V C0603
C116 100nF C0402 X5R 10V
C117 100nF C0402 X5R 10V
C118 100nF C0402 X5R 10V
C119 10uF X5R 6.3V C0603
C120 100nF C0402 X5R 10V
C121 100nF C0402 X5R 10V
C122 100nF C0402 X5R 10V


eMMC_DATA_STROBE/FLASH_CLE
eMMC_DATA_STROBE/FLASH_CLE
R29 1 2 0R 5% eMMC_DATA_STROBE
R0402
eMMC_CLKOUT/FLASH_DQS
eMMC_CLKOUT/FLASH_DQS
R30 1 2 0R 5% eMMC_CLKOUT
R0402
eMMC_RSTn/FSPI_D2/FLASH_WPn
eMMC_RSTn/FSPI_D2/FLASH_WPn
R31 1 2 NC 5% eMMC_RSTn
R0402
C123
NC
C0402
X5R
10V
eMMC_CMD/FLASH_WRn
eMMC_CMD/FLASH_WRn
R32 1 2 0R 5% eMMC_CMD
R0402
VCC_3V3
VCC3V3_FLASH
R34 1 2 0R 1%
R0603
VCC_1V8
R33 1 2 0R 1%
R0603
VCCIO_FLASH
VCCIO_FLASH
R35 1 2 10K 5% R0402
U3A
eMMC_D0/FLASH_D0
eMMC_D1/FLASH_D1
eMMC_D2/FLASH_D2
eMMC_D3/FLASH_D3
eMMC_D4/FLASH_D4
eMMC_D5/FLASH_D5
eMMC_D6/FLASH_D6
eMMC_D7/FLASH_D7
DATA0 A3
DATA1 A4
DATA2 A5
DATA3 B2
DATA4 B3
DATA5 B4
DATA6 B5
DATA7 B6
R36 1 2 10K 5% R0402
eMMC_CMD
CMD M5
eMMC_CLKOUT
CLK M6
R37 1 2 10K 5% R0402
eMMC_RSTn
RST_n K5
C132 2 1 4.7uF X5R C0402 10V
VDDi C2
eMMC_DATA_STROBE
Data Strobe H5
R38 NC R0402 5%
VSF1 E9
VSF2 E10
VSF3 F10
VSF4 K10
VCCQ1 C6
VCCQ2 M4
VCCQ3 N4
VCCQ4 P3
VCCQ5 P5
VCC1 E6
VCC2 F5
VCC3 J10
VCC4 K9
VSS1 J5
VSS2 A6
VSS3 C4
VSS4 E7
VSS5 G5
VSS6 H10
VSSQ1 K8
VSSQ2 N2
VSSQ3 N5
VSSQ4 P4
VSSQ5 P6
C125 100nF X5R 10V C0402
C126 100nF X5R 10V C0402
C127 100nF X5R 10V C0402
C128 100nF X5R 10V C0402
C124 4.7uF X5R 10V C0603
VCC3V3_FLASH
C130 100nF X5R 10V C0402
C131 100nF X5R 10V C0402
C129 4.7uF X5R 10V C0603
EMMC_B153_2L
BGA153_13RX11R5X0R9_2L
KLMBG2JETD-B041
SDINBDA6-32G-XI1
U3B
RFU1 A7
RFU2 E5
RFU3 E8
RFU4 G3
RFU5 G10
RFU6 K6
RFU7 K7
RFU8 P7
RFU9 P10
NC2 A2
NC8 A8
NC9 A9
NC10 A10
NC11 A11
NC12 A12
NC13 A13
NC14 A14
NC15 B1
NC21 B7
NC22 B8
NC23 B9
NC24 B10
NC25 B11
NC26 B12
NC27 B13
NC28 B14
NC29 C1
NC31 C3
NC35 C7
NC36 C8
NC37 C9
NC38 C10
NC39 C11
NC40 C12
NC41 C13
NC42 C14
NC43 D1
NC44 D2
NC45 D3
NC46 D4
NC54 D12
NC55 D13
NC56 D14
NC57 E1
NC58 E2
NC59 E3
NC68 E12
NC69 E13
NC70 E14
NC71 F1
NC72 F2
NC73 F3
NC82 F12
NC83 F13
NC84 F14
NC85 G1
NC86 G2
NC96 G12
NC97 G13
NC98 G14
NC196 P14
NC195 P13
NC194 P12
NC193 P11
NC191 P9
NC190 P8
NC184 P2
NC183 P1
NC182 N14
NC181 N13
NC180 N12
NC179 N11
NC178 N10
NC177 N9
NC176 N8
NC175 N7
NC174 N6
NC171 N3
NC169 N1
NC168 M14
NC167 M13
NC166 M12
NC165 M11
NC164 M10
NC163 M9
NC162 M8
NC161 M7
NC157 M3
NC156 M2
NC155 M1
NC154 L14
NC153 L13
NC152 L12
NC143 L3
NC142 L2
NC141 L1
NC140 K14
NC139 K13
NC138 K12
NC129 K3
NC128 K2
NC127 K1
NC126 J14
NC125 J13
NC124 J12
NC115 J3
NC114 J2
NC113 J1
NC112 H14
NC111 H13
NC110 H12
NC101 H3
NC100 H2
NC99 H1
EMMC_B153_2L
VCC_3V3
R39 10K 5%
Maskrom_key-
SW2
Maskrom_key+
eMMC_D0/FLASH_D0
Q1 S8050 SOT_23
R40 47K R0402 5%

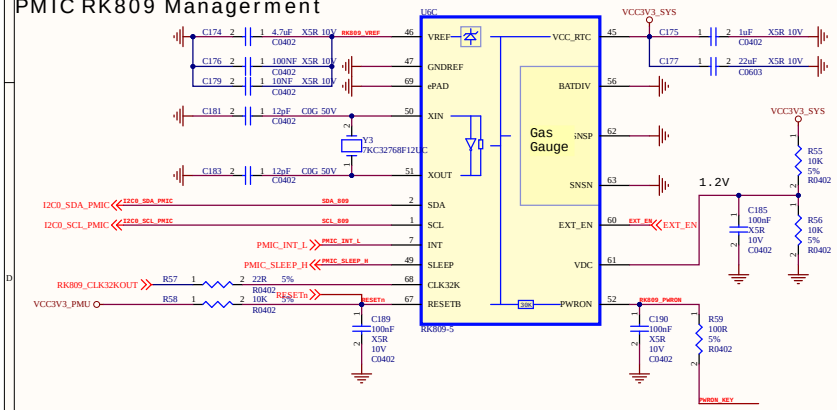


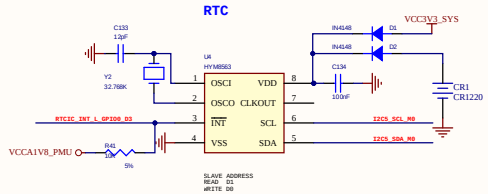
PMIC RK809 DCDC



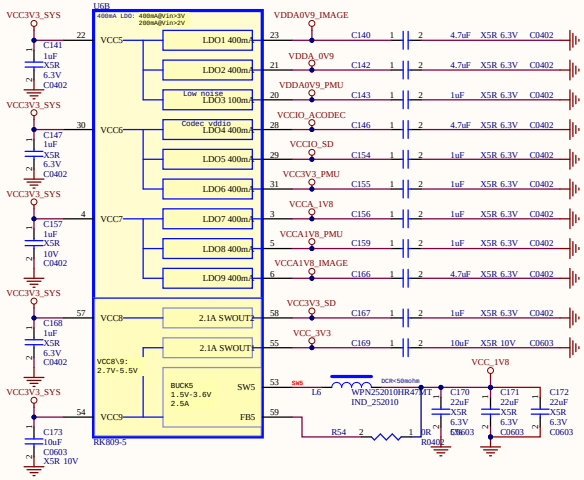
DDR4	1.21V	62K 1%
LPDDR4/4x	1.11V	47K 1%
DDR3	1.53V	110K 1%
DDR3L	1.35V	82K 1%
LPDDR3	1.25V	68K 1%

PMIC RK809 Managerment

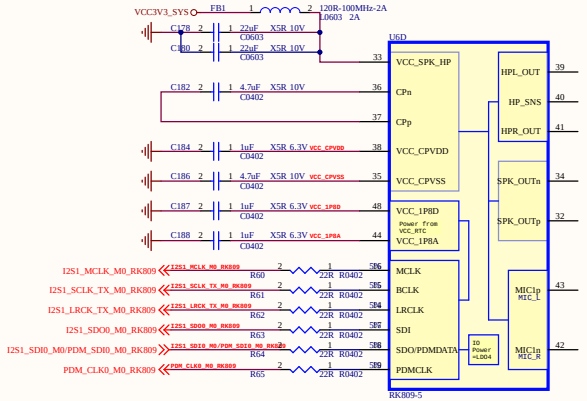




PMIC RK809 LDO



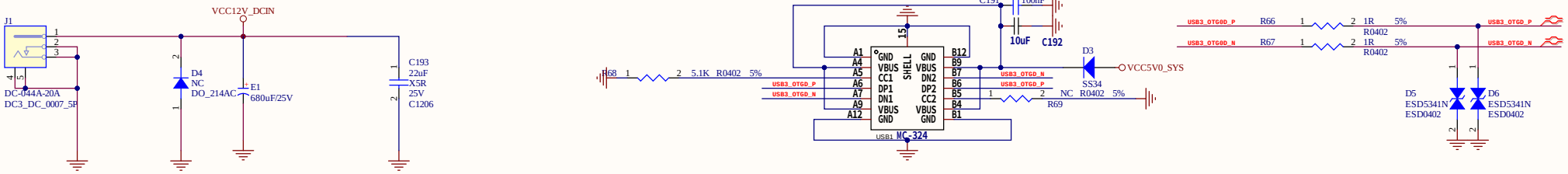
PMIC RK809 CODEC



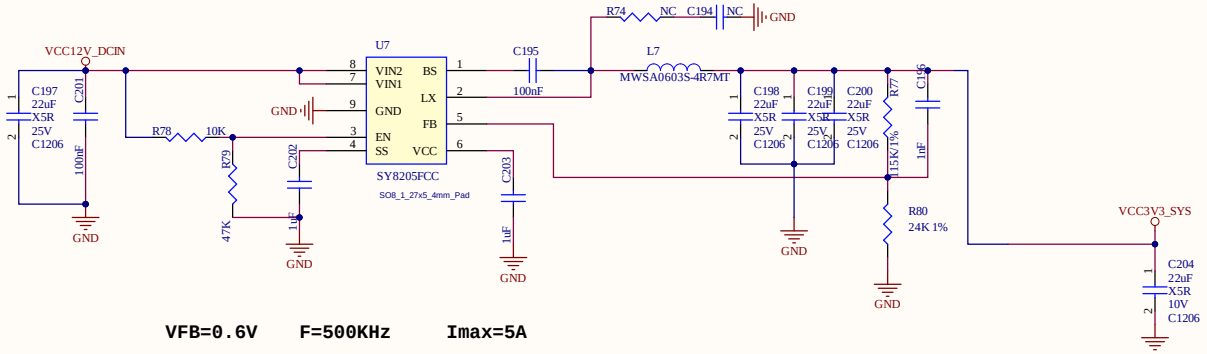
12V/3A DCIN

Note:

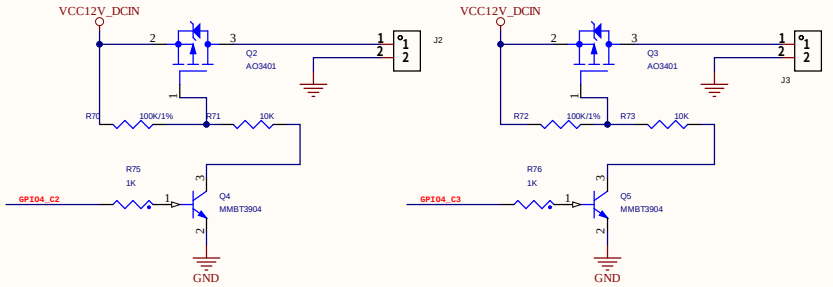
With SATA,PCIe, the current is estimated according to the actual number of SATA,PCIe



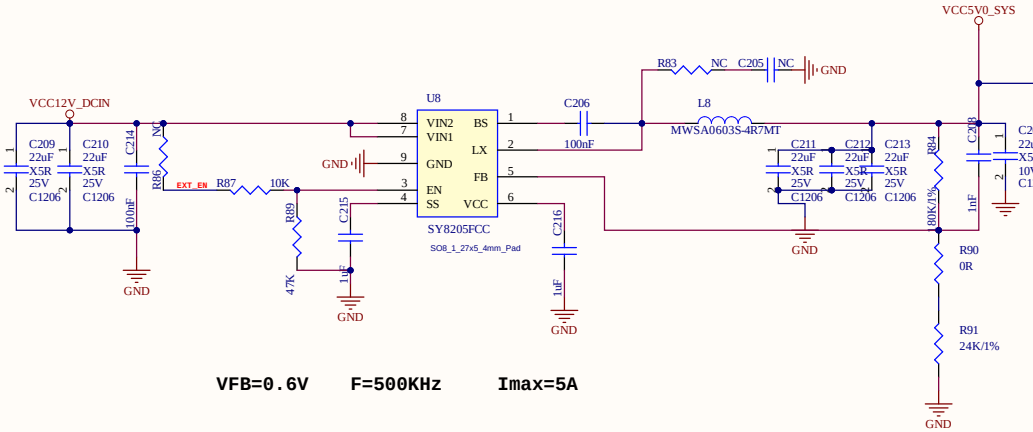
VCC3V3_SYS



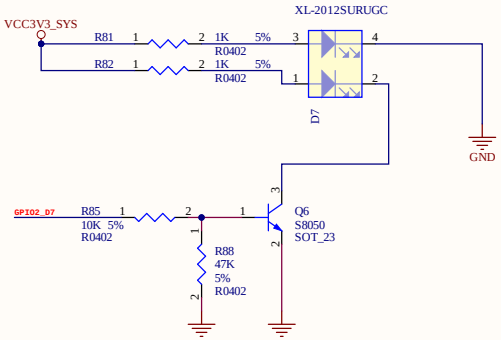
VFB=0.6V F=500KHz Imax=5A



VCC5V0_SYS



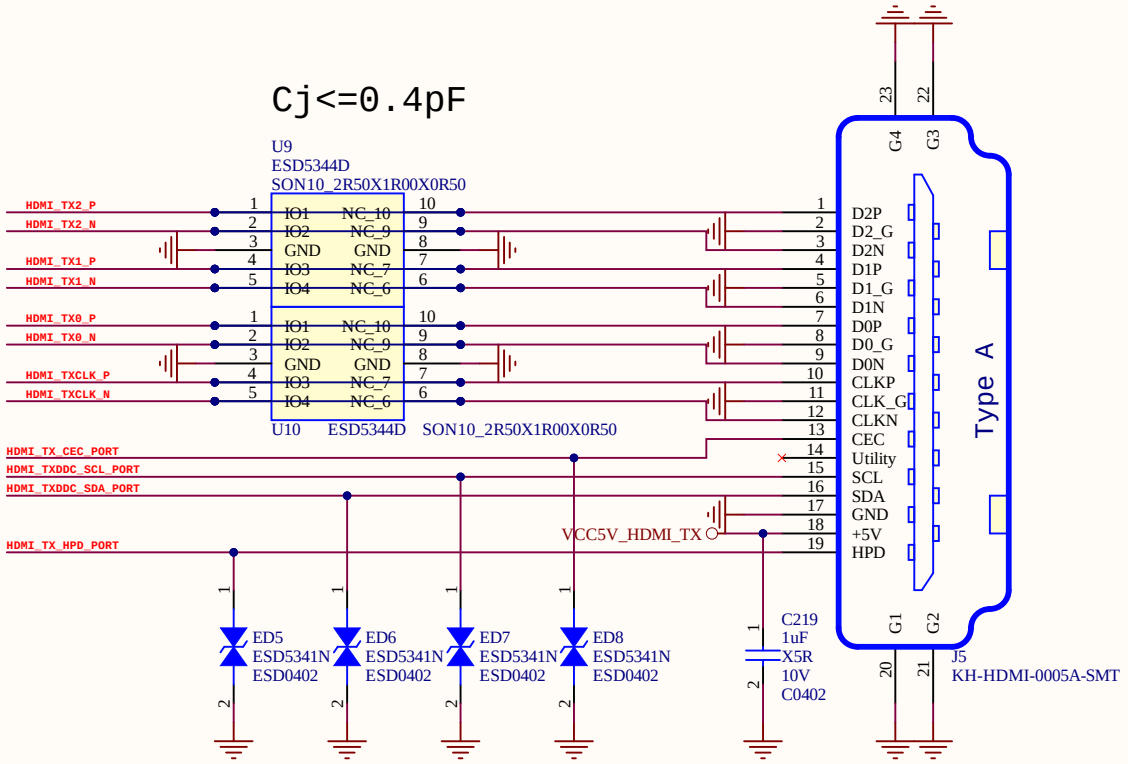
VFB=0.6V F=500KHz Imax=5A



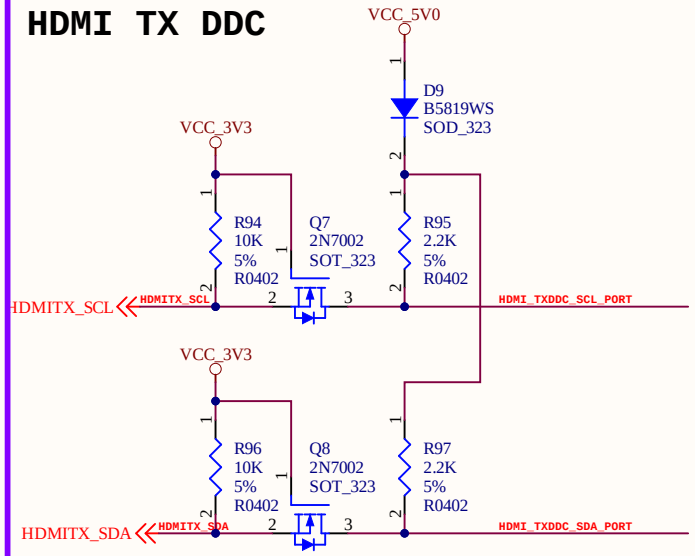

USB3_OTG0_VBUSDET
R92
1
2
10K
5%
R0402
VCC5V0_USB
R93
10K
5%
R0402
C217
22uF
VCC5V0_USB
C218
100nF
ESD0402
ESD5341N
ED1
USB2_HOST3D_N
USB2_HOST3D_P
ED2
ESD5341N
ESD0402
VBUS
D-
D+
GND
VBUS
D-
D+
GND
GND
GND
GND
ESD0402
ESD5341N
ED3
USB2_HOST2D_N
USB2_HOST2D_P
ED4
ESD5341N
ESD0402

HDMI2.0 TX

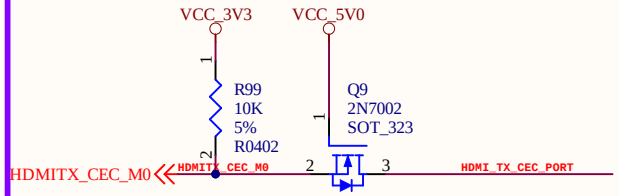
Cj<=0.4pF



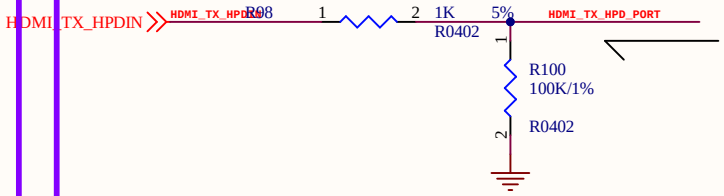
HDMI TX DDC

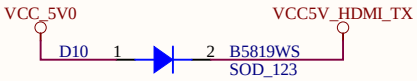


HDMI TX CEC

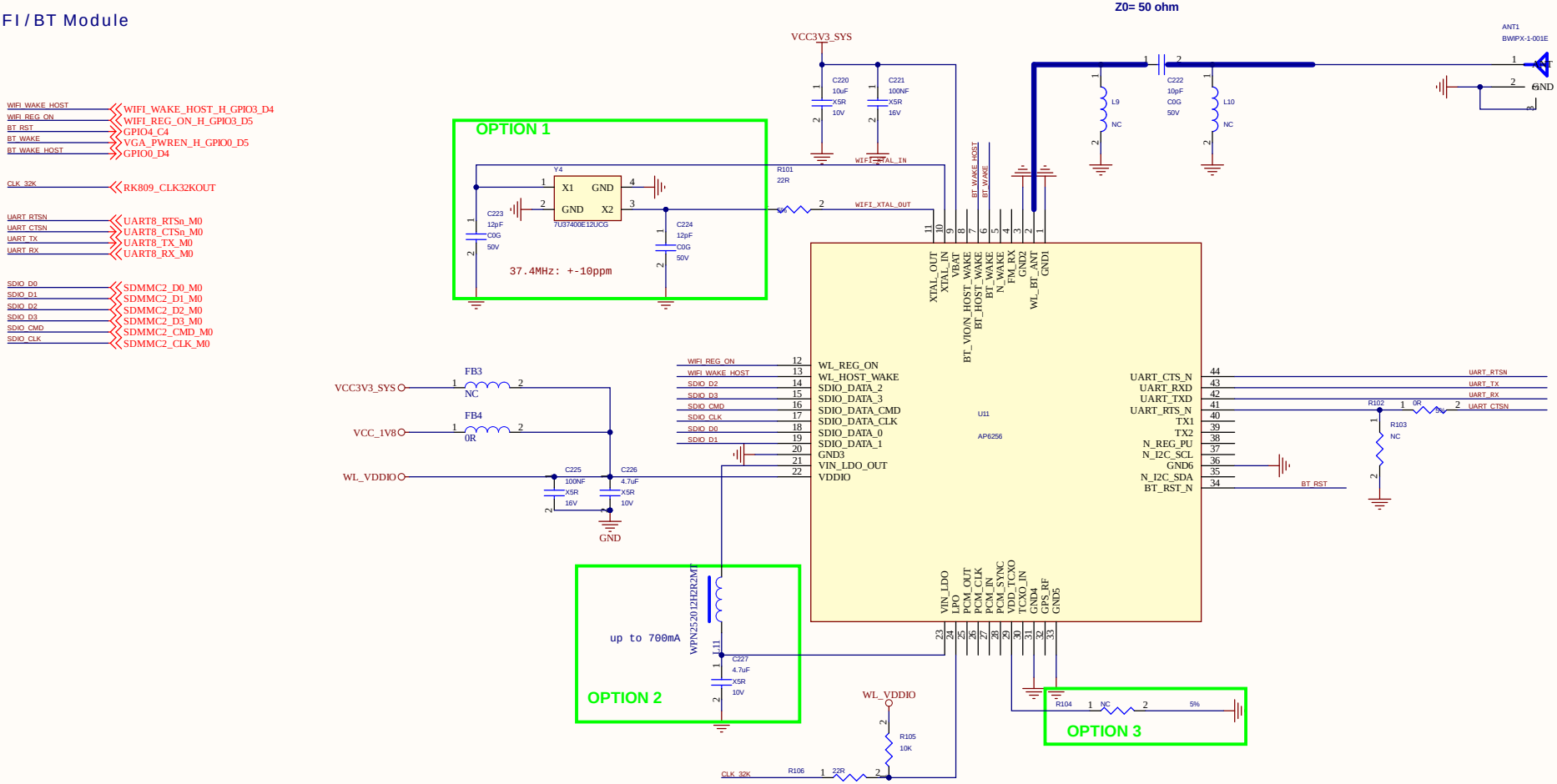


HDMI TX HPD

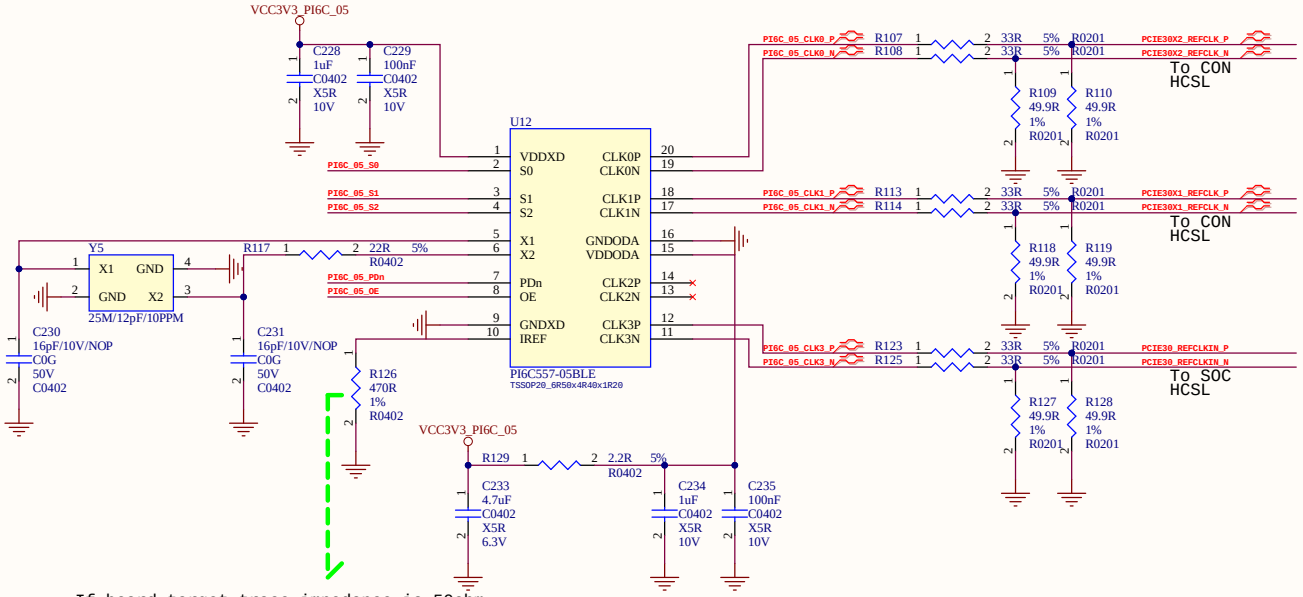




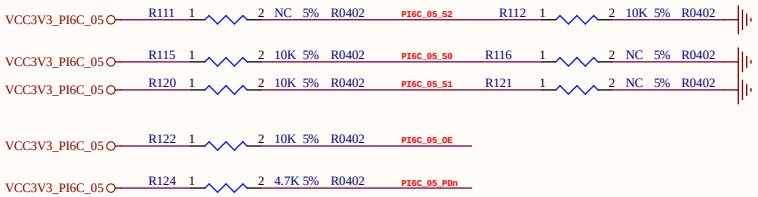
WIFI/BT Module

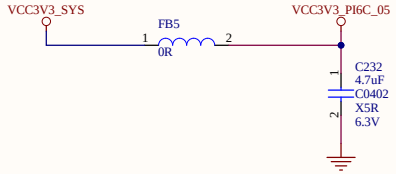


OPTION	WIFI				BT	Crystals	VCCIO_SDIO	OPTION1	OPTION2	OPTION3
	a	b/g/n	ac	5GHz						
AW-CM256SM	Yes	Yes	Yes	Yes	4.2	37.4MHz	1.71-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0
AP6236/AP6212	No	Yes	No	No	4.2/4.0	26MHz	1.71-3.63V	Yes	Yes	No
AP6256/AP6255	Yes	Yes	Yes	Yes	5.0/4.2	37.4MHz	1.62-3.63V	Yes	Yes	Yes@SDIO2.0 No@SDIO3.0

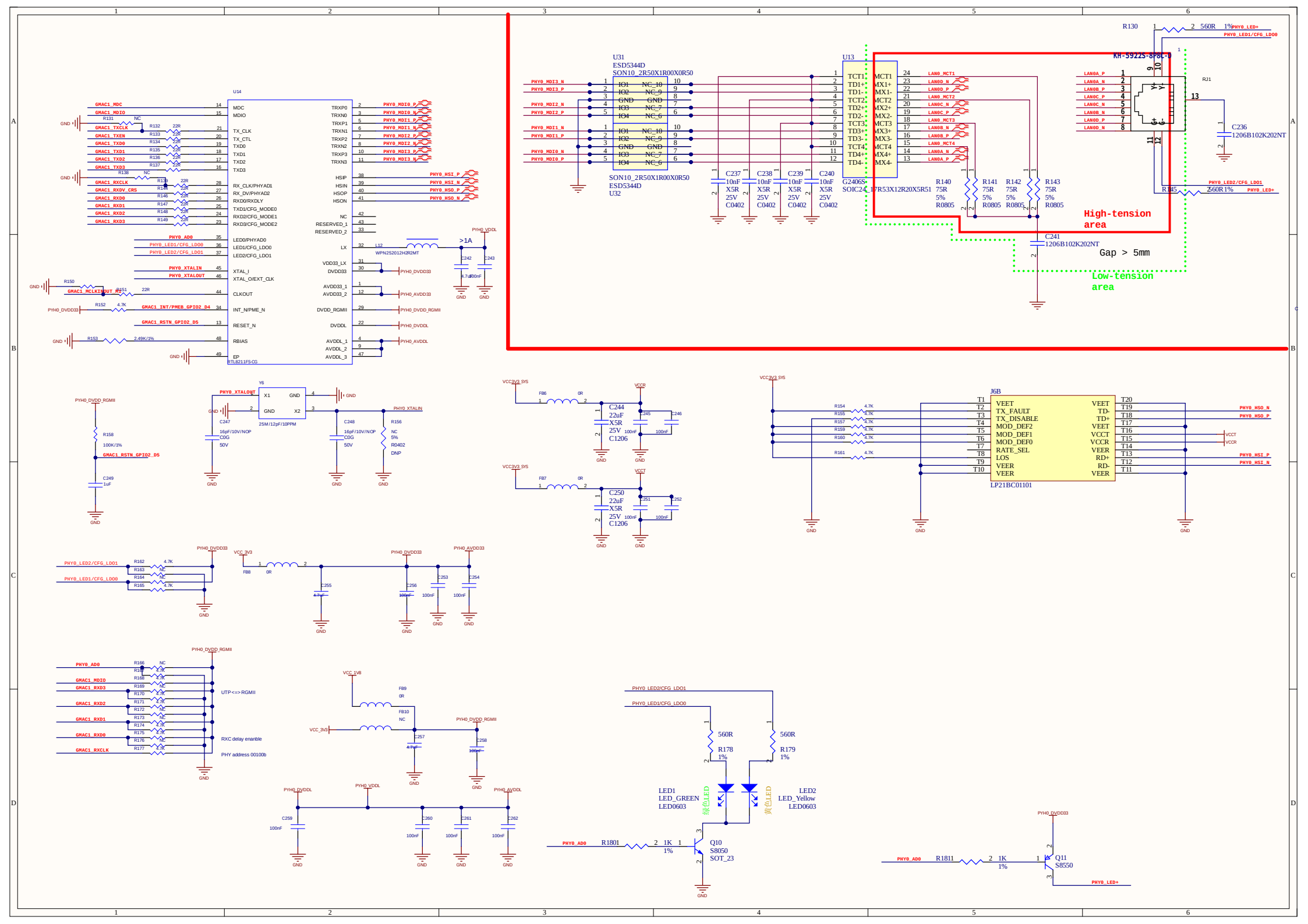


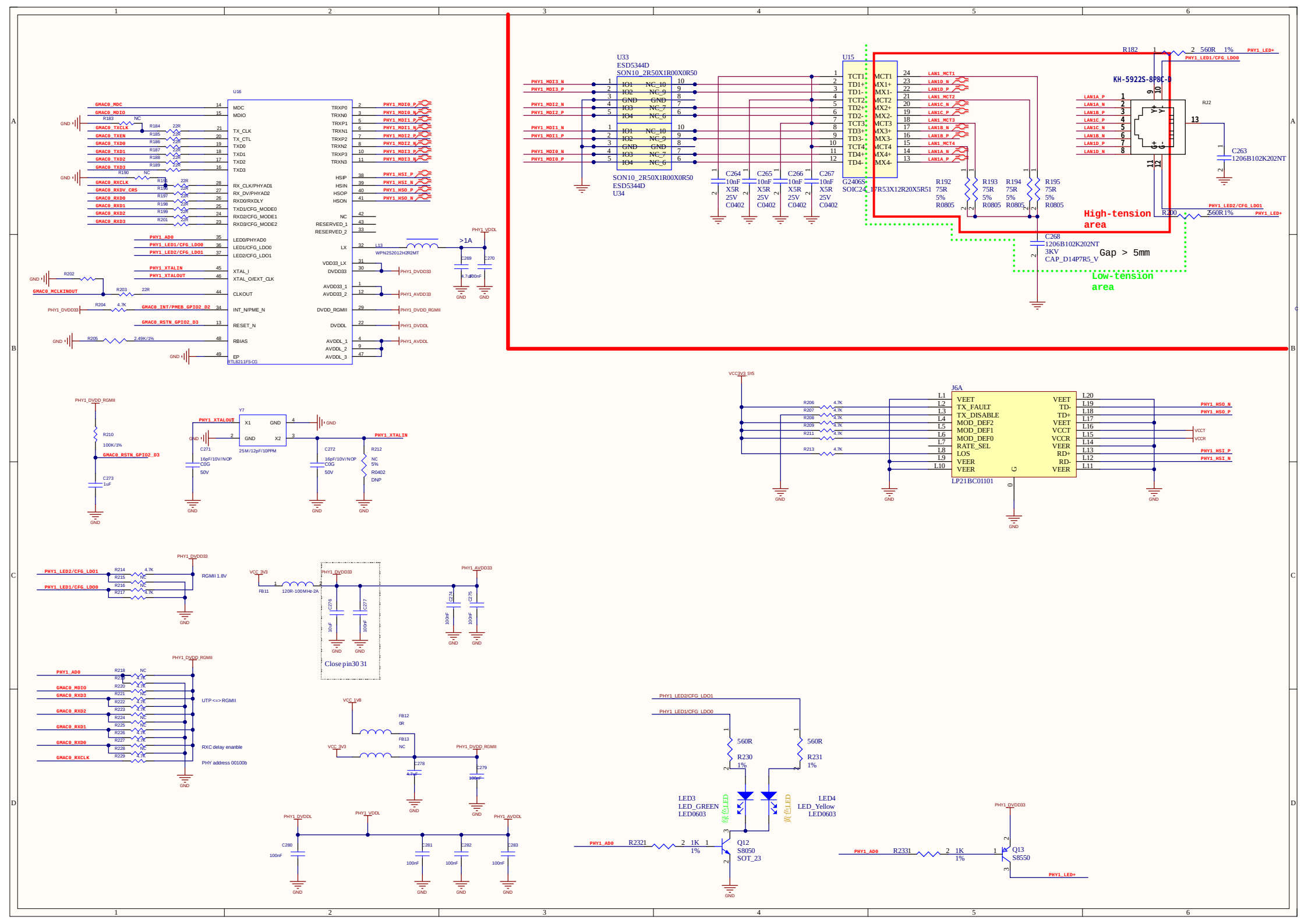
PI6C_S2	PI6C_S1	PI6C_S0	Spread %	Out Freq
0	0	0	-0.5	100MHz
0	0	1	-1.0	100MHz
0	1	0	-1.5	100MHz
0	1	1	No Spread	100MHz



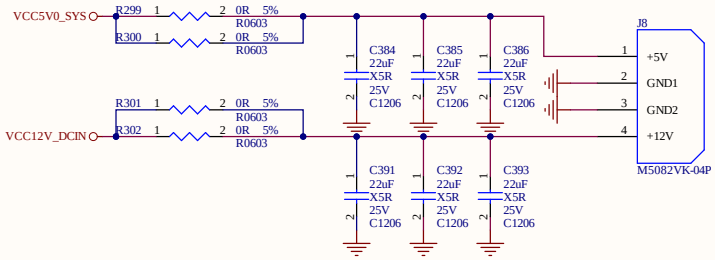


If board target trace impedance is 50ohm
then R = 475ohm providing an IREF of 2.32 mA . The output current (IOH) is 6 * IREF .
6x2.32X50=696mV


U14
RTL8211FS-CG
U31
ESD5344D
SON10_2R50X1R00X0R50
U32
U13
G2406S
SOIC24_17R53X12R20X5R51
KH-5922S-878C-B
RJ1
High-tension area
Low-tension area
Gap > 5mm
J6B
LP21BC01101
Y6
25M/12pF/10PPM
L12
WPN252012H2R2MT
Q10
S8050
SOT_23
Q11
S8550
LED1
LED_GREEN
LED0603
LED2
LED_Yellow
LED0603
UTP<=> RGMII
RXC delay enanble
PHY address 00100b

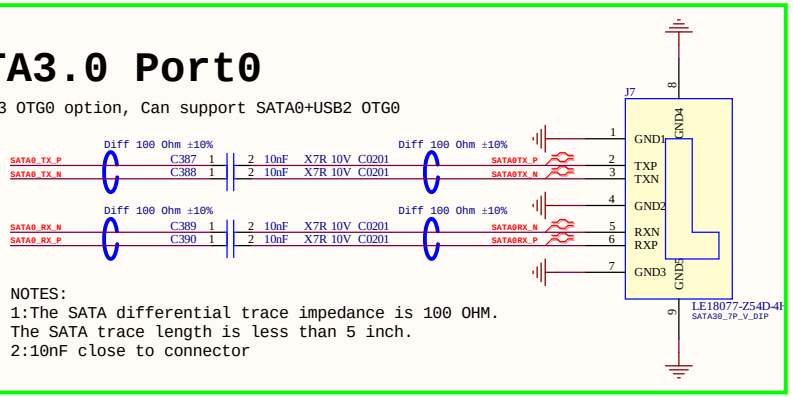

U16
RTL8211FS-CG
U33
ESD5344D
SON10_2R50X1R00X0R50
U34
U15
G2406S
SOIC24_17R53X12R20X5R51
KH-5922S-8P8C-D
RJ2
High-tension area
Low-tension area
Gap > 5mm
J6A
LP21BC01101
Close pin30 31
LED3
LED_GREEN
LED0603
LED4
LED_Yellow
LED0603
Q12
S8050
SOT_23
Q13
S8550

SATA Power



SATA3.0 Port0

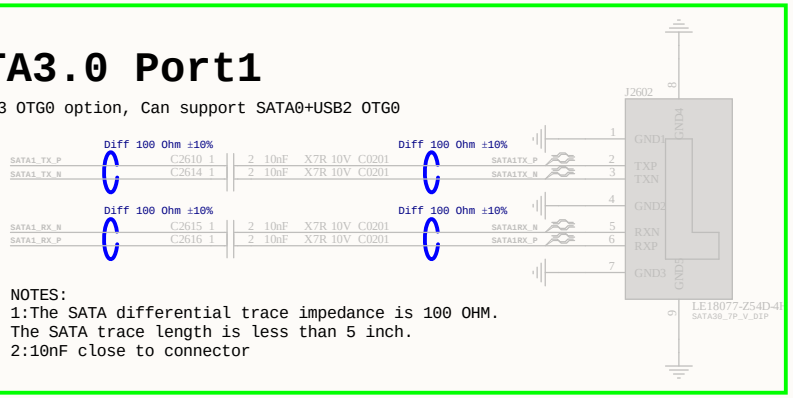
And USB3 OTG0 option, Can support SATA0+USB2 OTG0



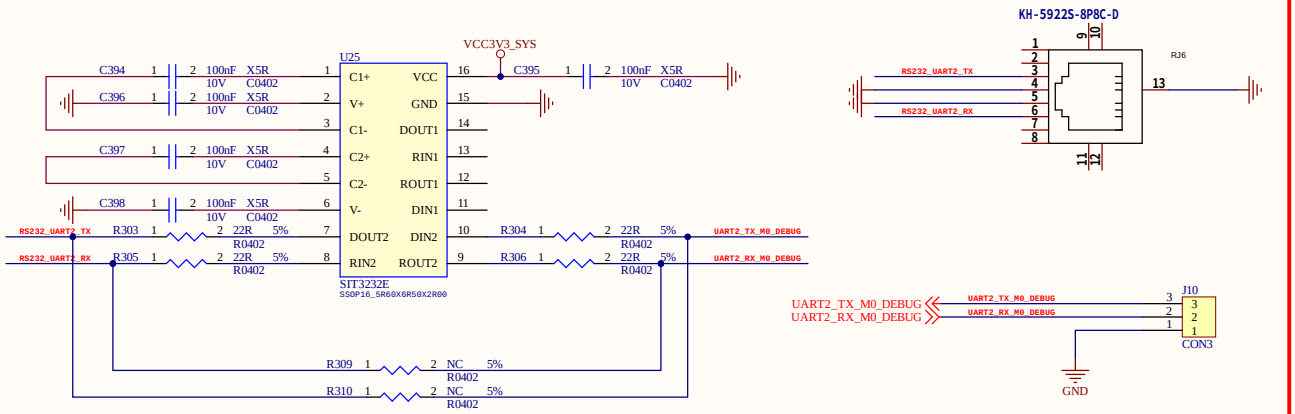
NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector

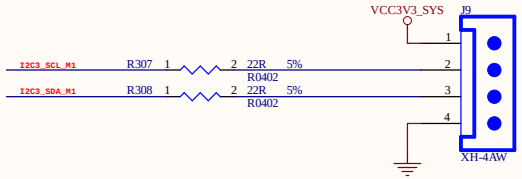
SATA3.0 Port1

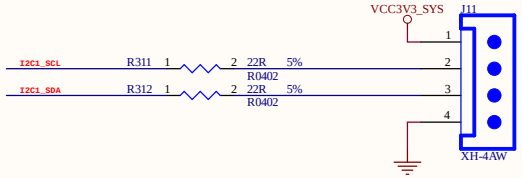
And USB3 OTG0 option, Can support SATA0+USB2 OTG0

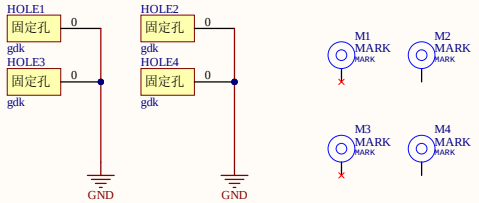


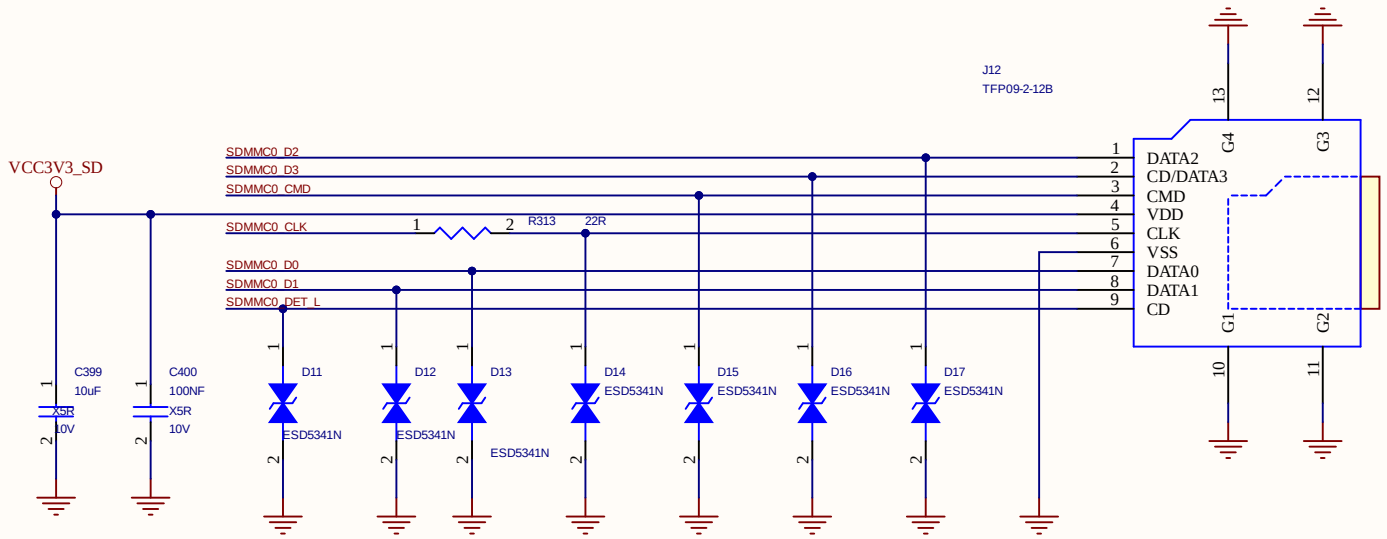
NOTES:
1:The SATA differential trace impedance is 100 OHM.
The SATA trace length is less than 5 inch.
2:10nF close to connector



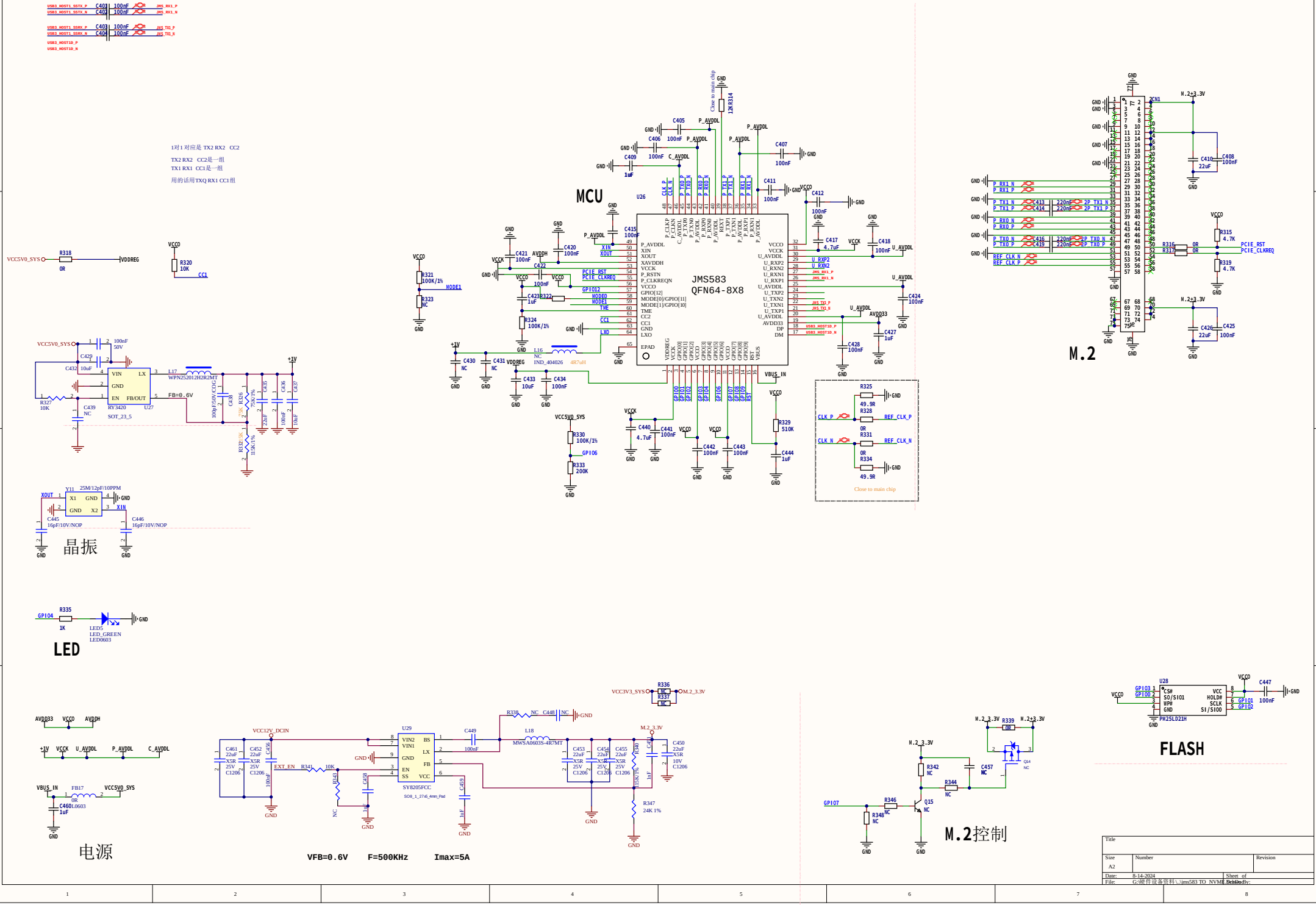








Shen Zhen RONGPIN ELECTRONICS CO.,LTD	
Title	RK3568 Board Schematics (TEL 0755-23036780)
Size: A	Document Number: TF/SATA
Rev: 1.0	
Date:	Sheet 5 of 14



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Board Stack Report